Low Power CMOS Process Technology

Scott Crowder

IBM, SRDC, East Fishkill, NY

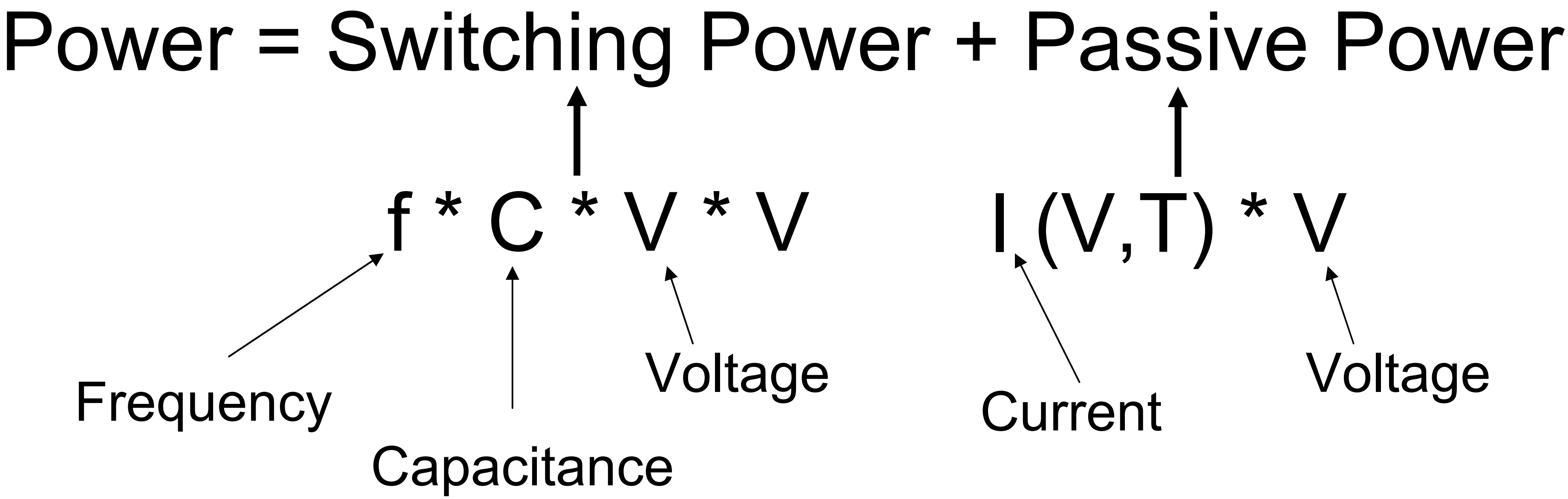
Outline

- What is Low Power?
- Process For Low Standby Power
- Process For Low Active Power
- Other Low Power Requirements
- Conclusions

Power Components in Digital CMOS

- Standby Power
  - Power when no function is occurring
  - Critical for battery driven
  - Can be reduced through circuit optimization
  - Temperature dependent leakage current dominates power
- Active Power
  - Switching power plus passive power
  - Critical for higher performance applications
- Other Sources of Power Consumption
  - Analog & I/O Power
    - Some circuit configurations have current flow even w/o switching
  - Dynamic Memory Refresh Power
    - eDRAM, 1T SRAM require periodic refresh of data

Power Components (simple version)



Power = Switching Power + Passive Power

f * C * V * V

I (V,T) * V

Frequency

Capacitance

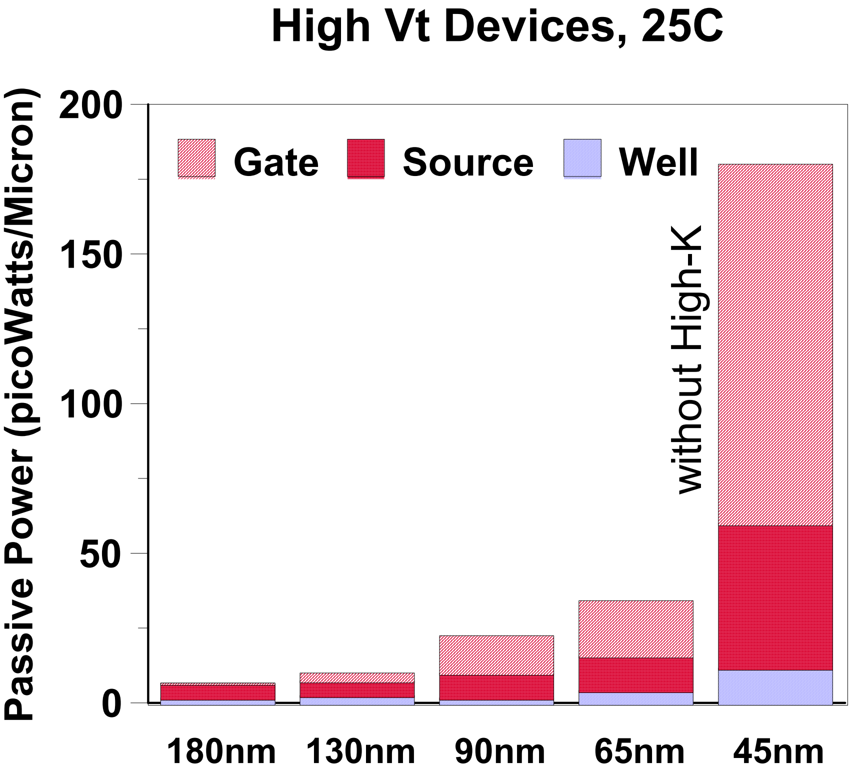
Voltage

Current

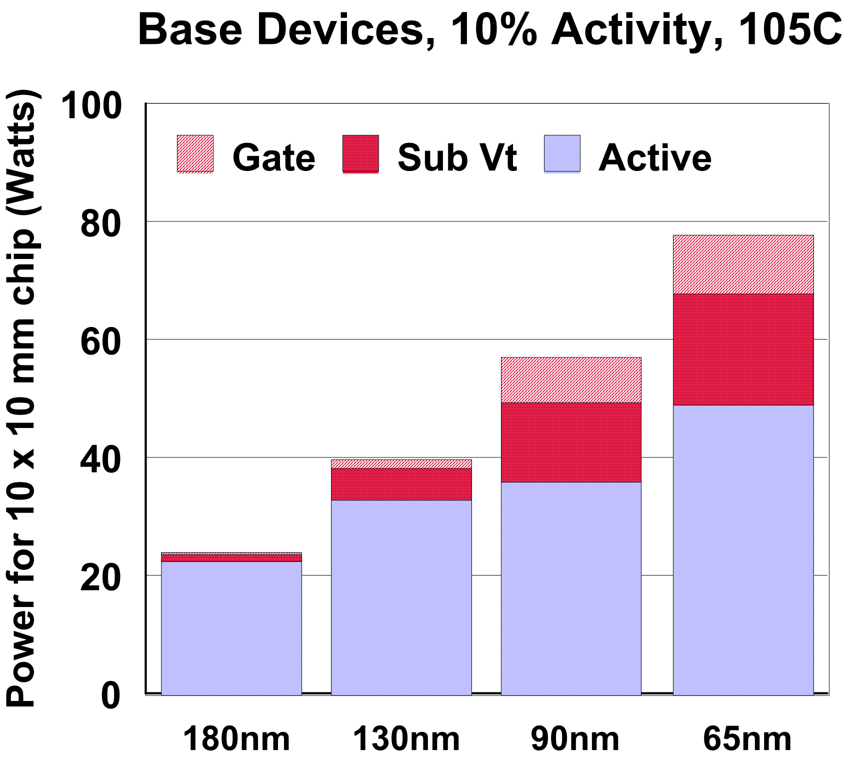
Voltage

Power Trends

Handheld Technology



Desktop Processor Technology



What is Low Power in CMOS?

- Depends on product application
- Examples
  - #1: Handheld phone chip
  - #2: Server microprocessor chip

Example #1: Handheld Application

- Key Attributes:
  - Battery Powered
  - In off-state significant portion of time
  - Standby condition at room temperature
  - Lawsuit if chip gets too hot
  - Standby dominates power requirements
    - Leakage current at room temperature dominates power

- What is Low Power Optimized Design?
  - Want highest performance @ given leakage current

Example #2: Server Application

- Key Attributes:
  - Powered by electrical grid
  - Almost always on
  - Power condition at operating temperature
  - Lower power reduces packaging & cooling expense
  - Switching power dominated power requirements in past
    - Want lower capacitance, voltage at maximum frequency
  - Passive power at operating temperature now a major component
    - Want lower high temperature leakage current & lower voltage

- What is Low Power Optimized Design?
  - Want switching power to dominate
  - Want to maximize performance & modulate voltage to meet power requirements

One More Major Component: Cost

- Critically important to technical solution

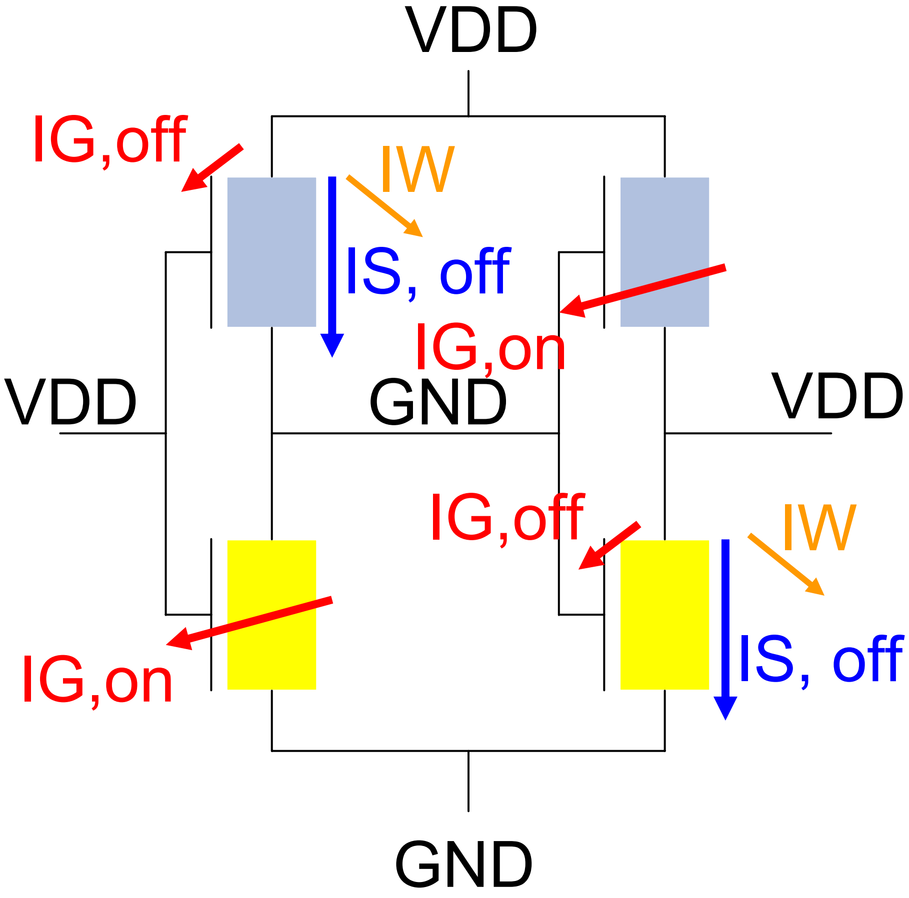
- Example #2: Server microprocessor
  - Higher performance = higher end product price
  - Will add reasonable cost to enable performance
    - Higher cost process: strain engineering, added metal levels
    - Flip-chip packaging, heat sinks & fans

- Example #1: Handheld application
  - Market will not allow higher cost solutions
  - Lower power specifications
  - Focus on lowest cost process that meets market demand

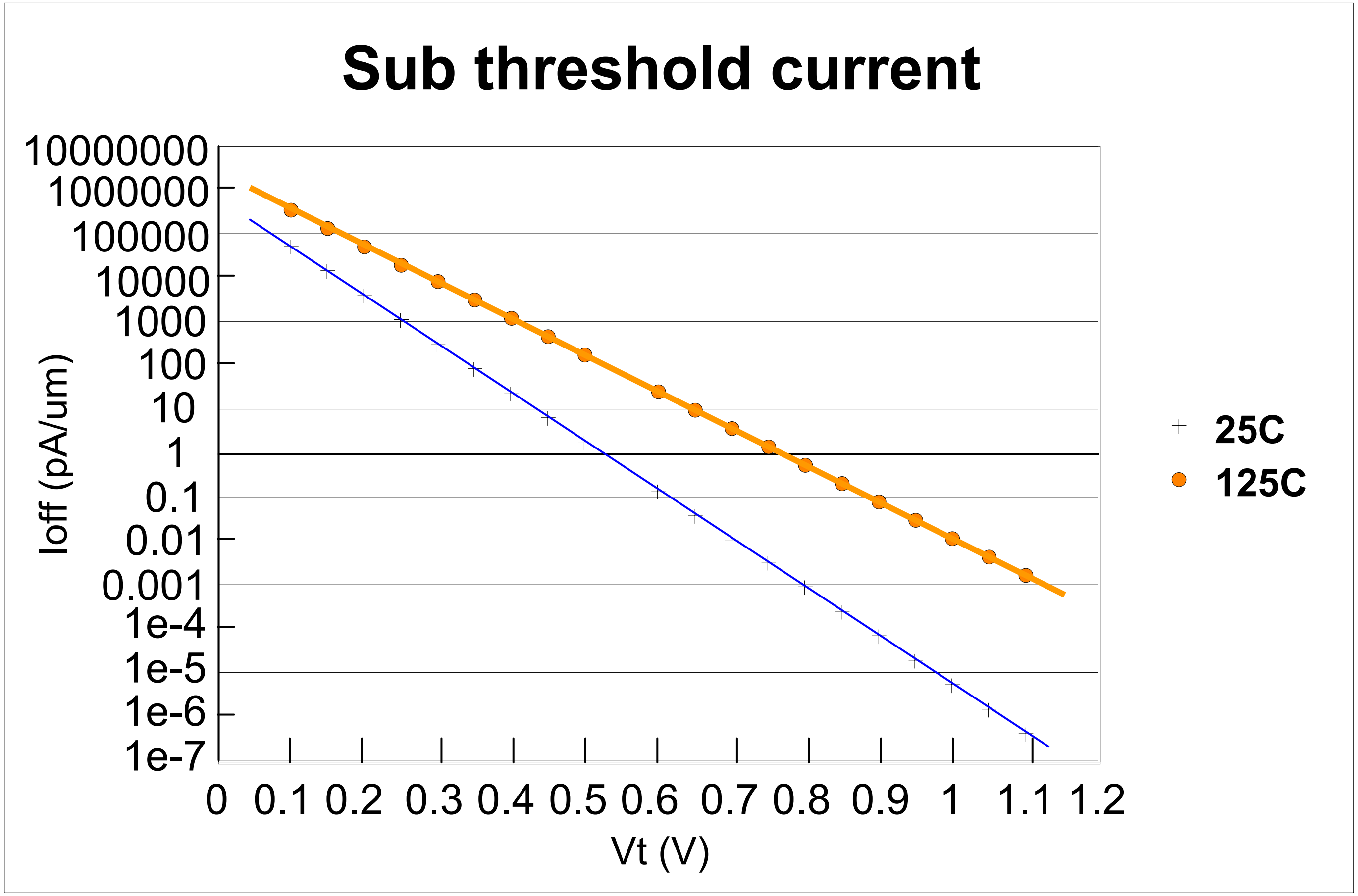
Low Standby Power

Components of Passive Power

- **Major components**
  - **Source leakage current**
    - **Sub threshold off-state current**
  - **Gate current**
    - **Tunneling current thru gate dielectric**
  - **Well current**
    - **Band-to-band tunneling current to well**

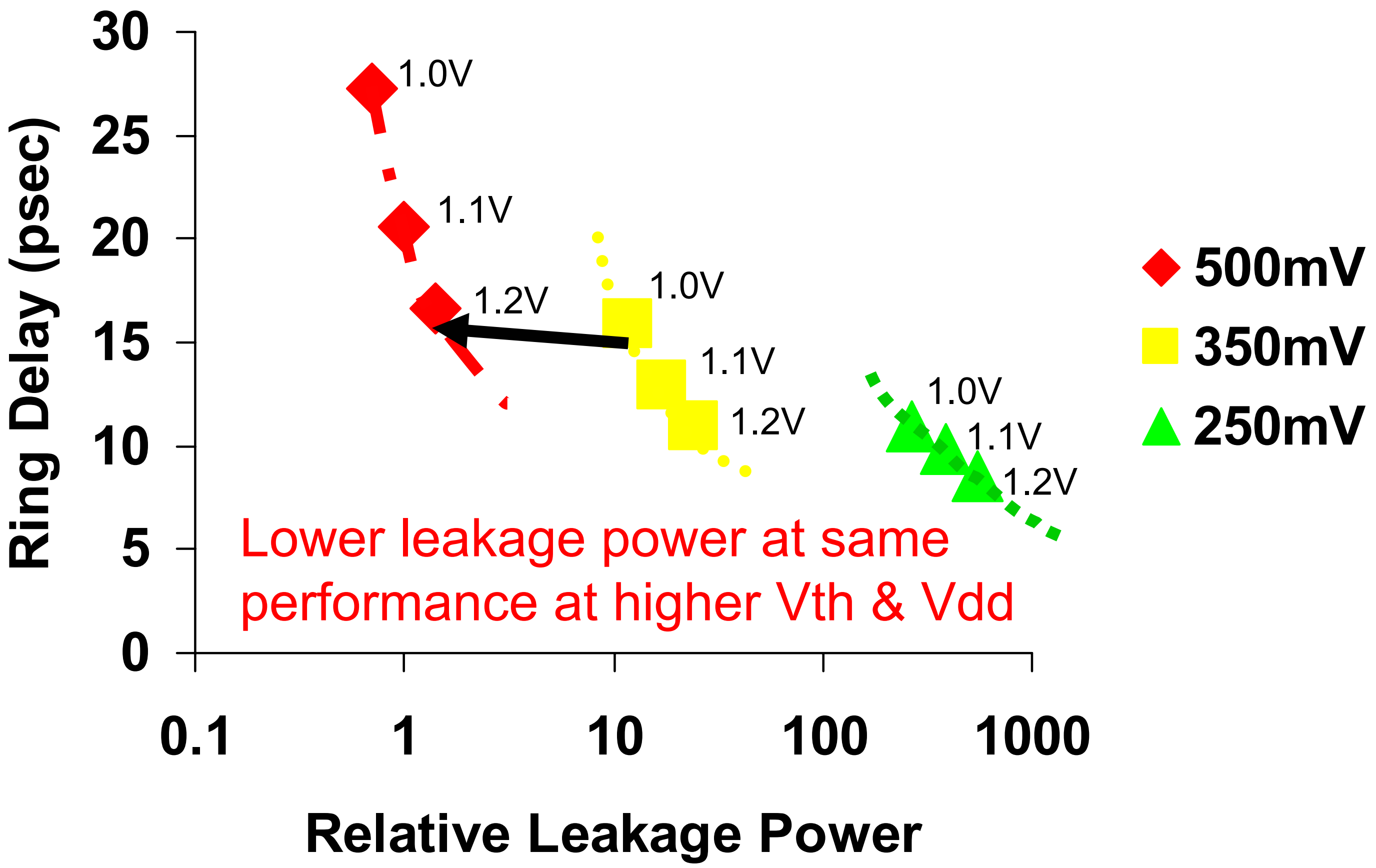


IS: Source Sub threshold Leakage



- **Strong Vth dependence**
- **Strong Temperature dependence**

Under scaling Supply Voltage

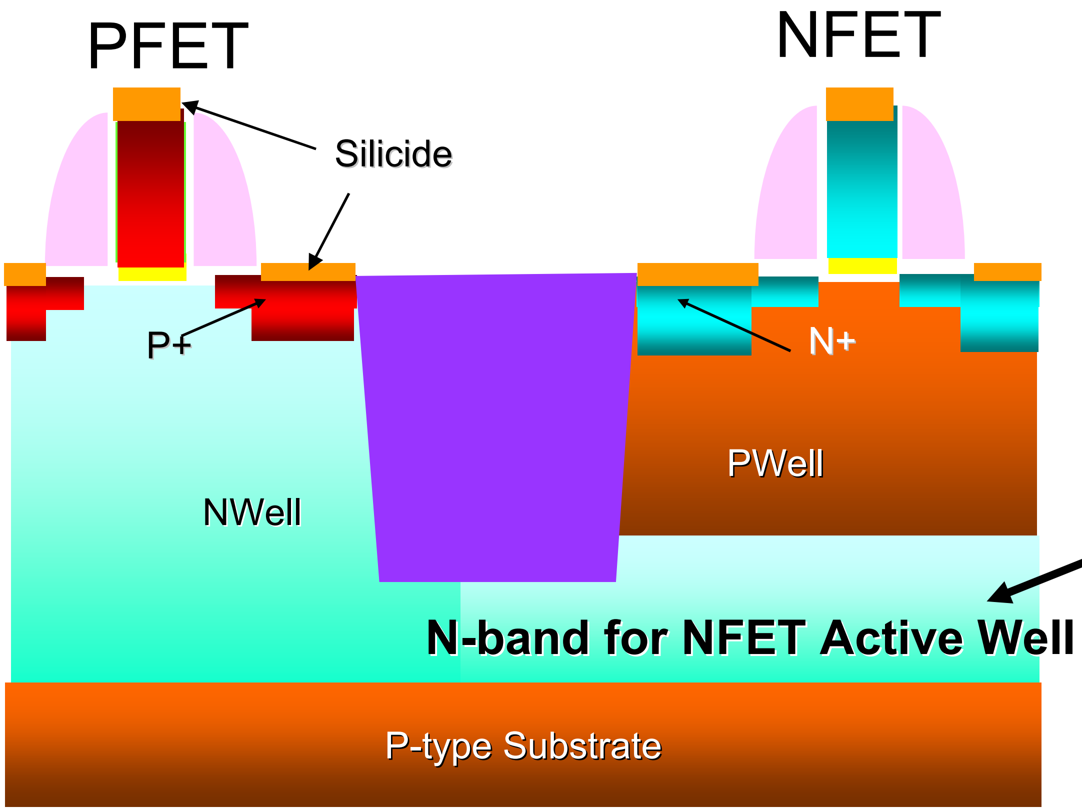


Lower leakage power at same performance at higher Vth & Vdd

- **Higher performance at given leakage power by raising Vdd**
- **Vdd scaling has slowed dramatically for low standby power**

Methods to Modulate IS Leakages

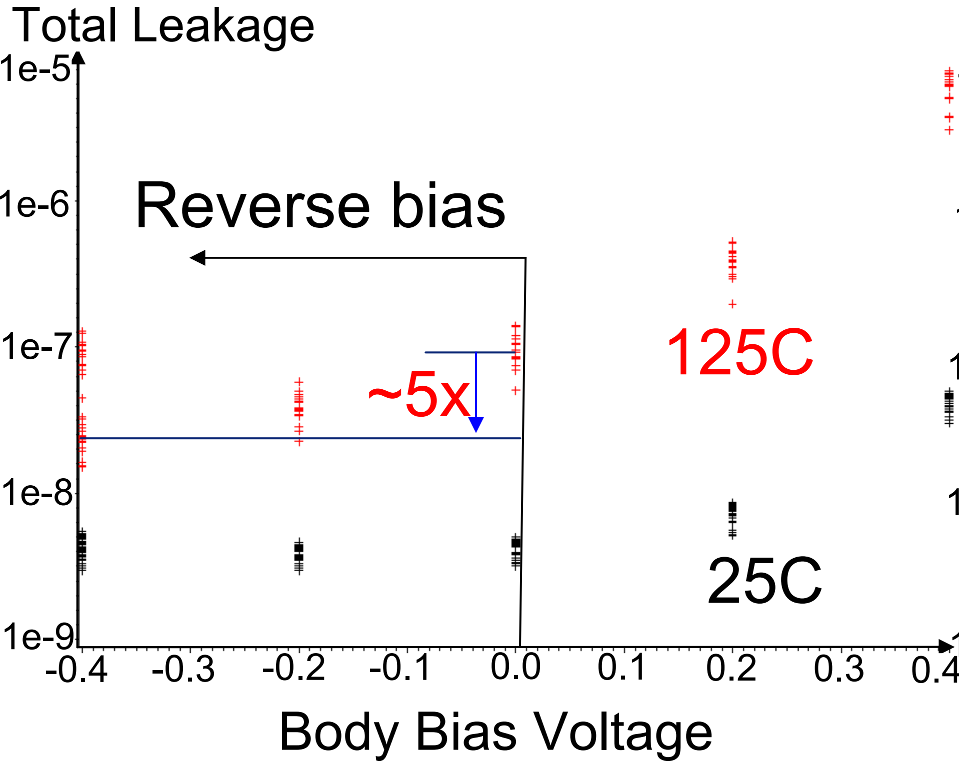
- Reverse Body Bias or Active Well



Added well implant to separate well and substrate

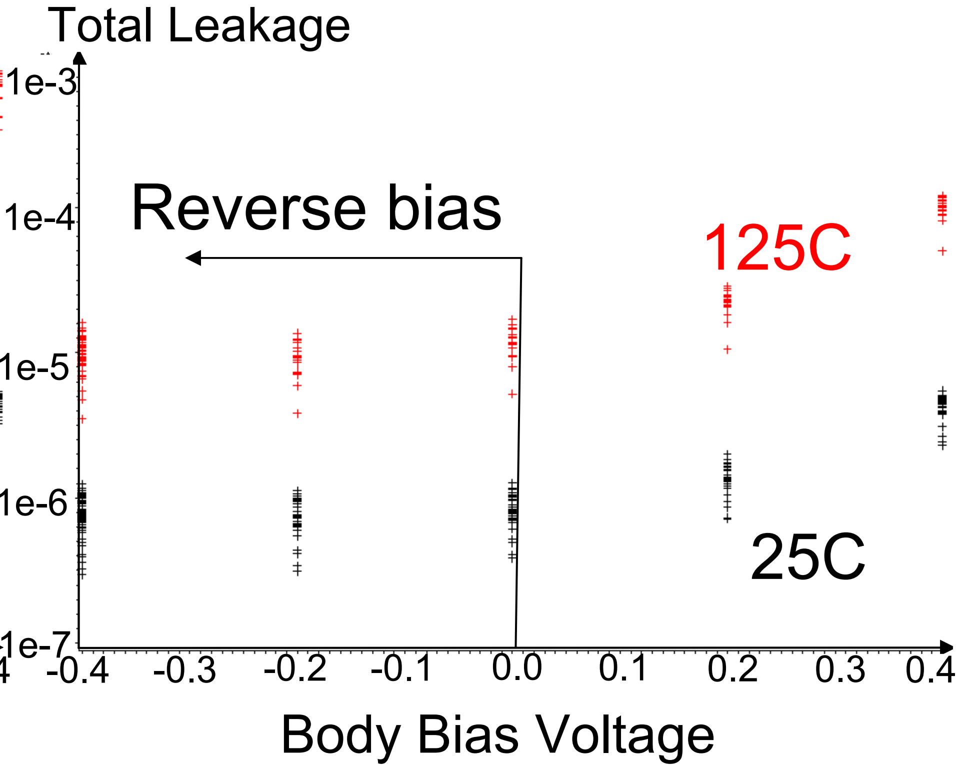
Reverse Body Bias

HIGH VT DEVICES



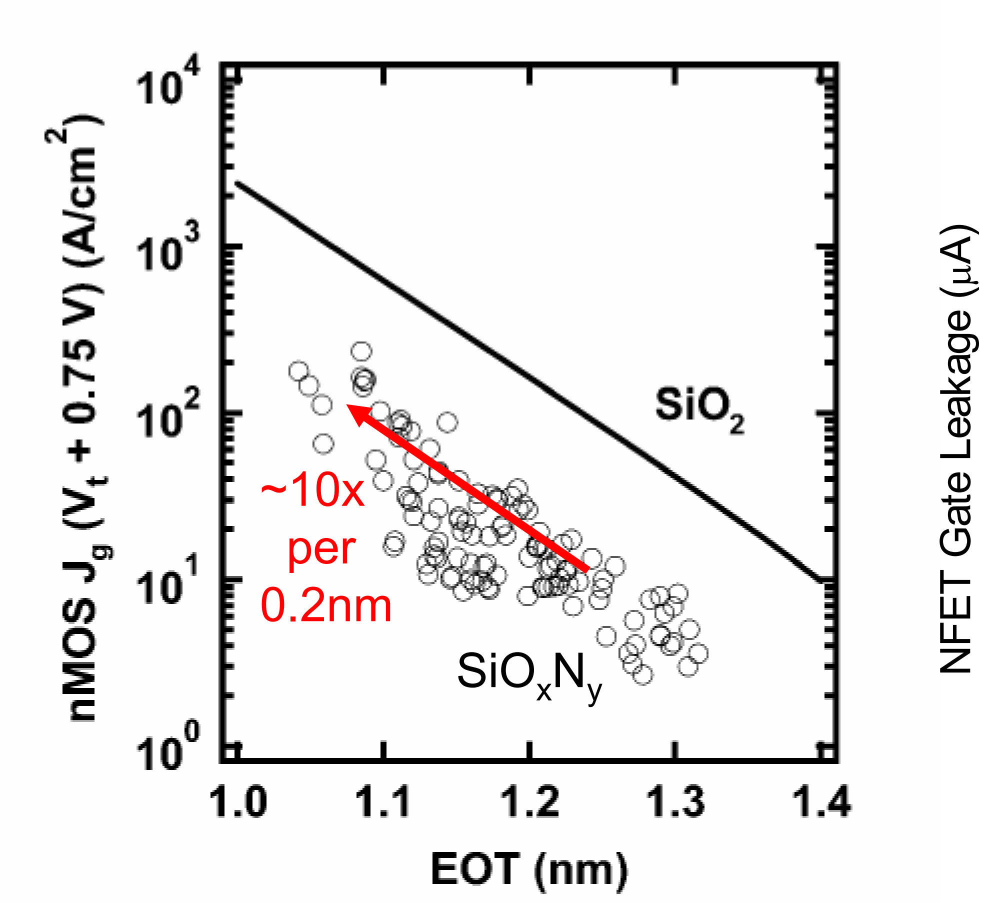
Body bias dependence limited by IG & IW leakage

LOW VT DEVICES

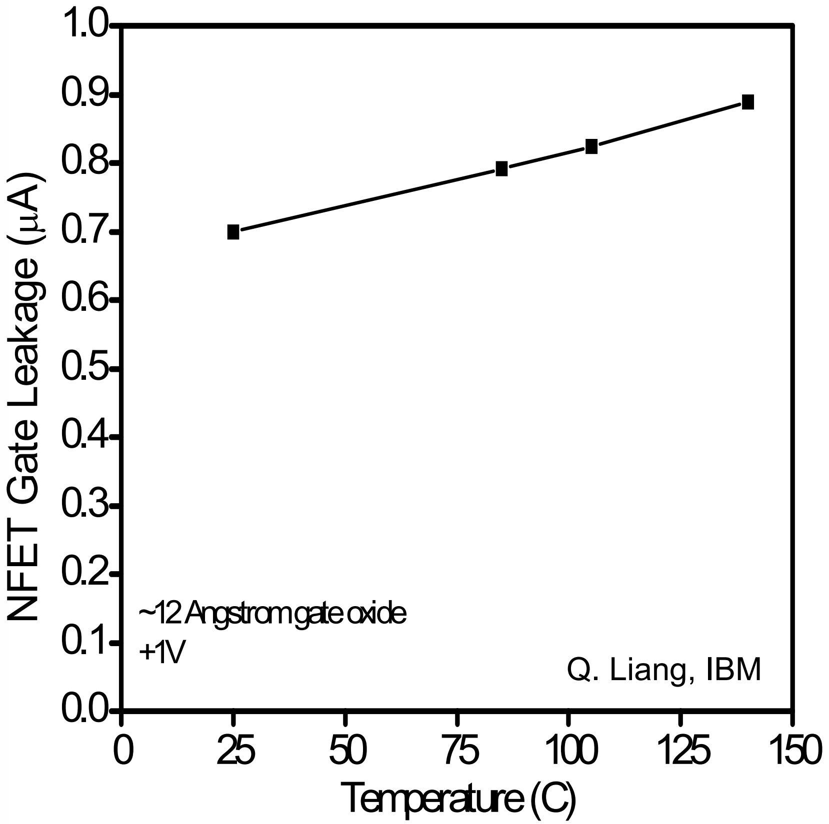


Leakage dominated by IS but low body effect

IG: Gate Leakage

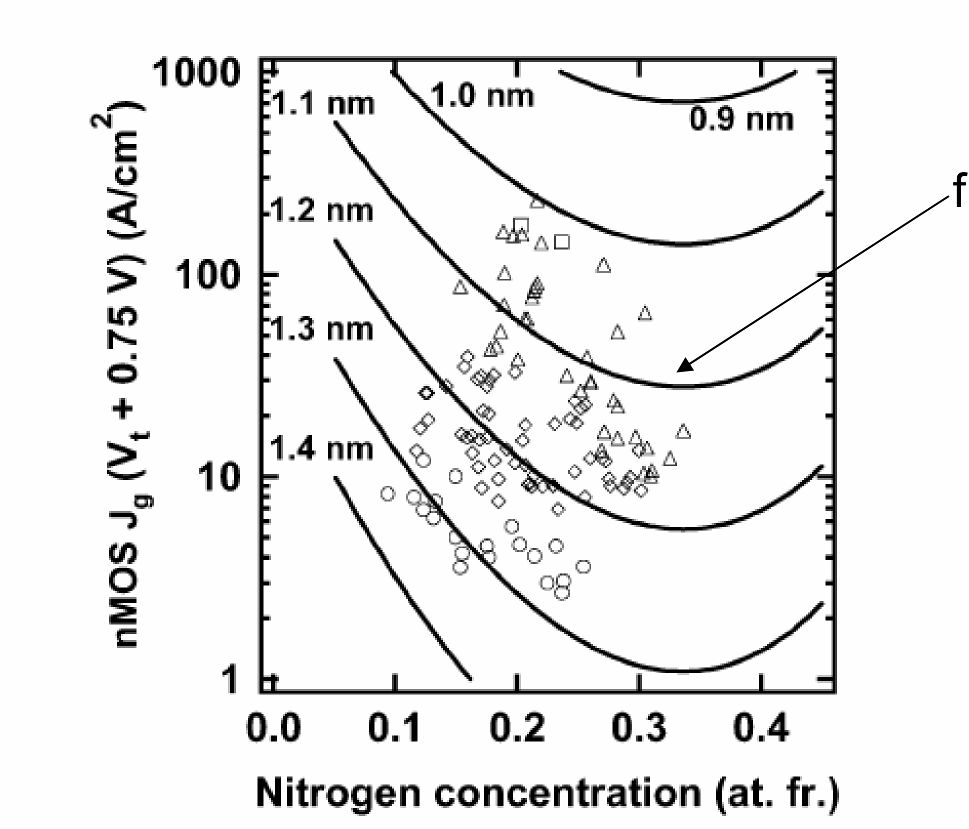


Kraus, et al, IEEE TED Vol 52, No. 6 2005, page 1141



- **Function of gate dielectric material and thickness**
- **Low temperature dependence -> dominates at low T**

Methods to Reduce Gate Leakage: N

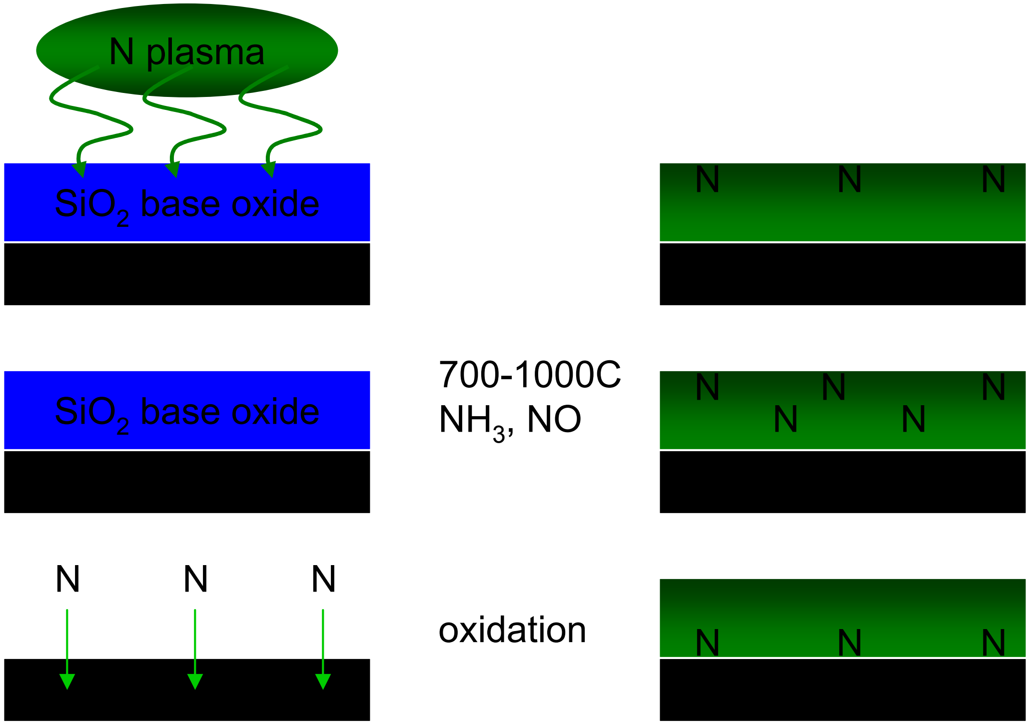


fixed EOT contours

Kraus, et al, IEEE TED Vol 52, No. 6 2005, page 1141

- Increased Nitrogen concentration reduces gate leakage

Methods to Incorporate Nitrogen



plasma nitridation

more N at top surface

thermal nitridation

700-1000C
NH_3, NO

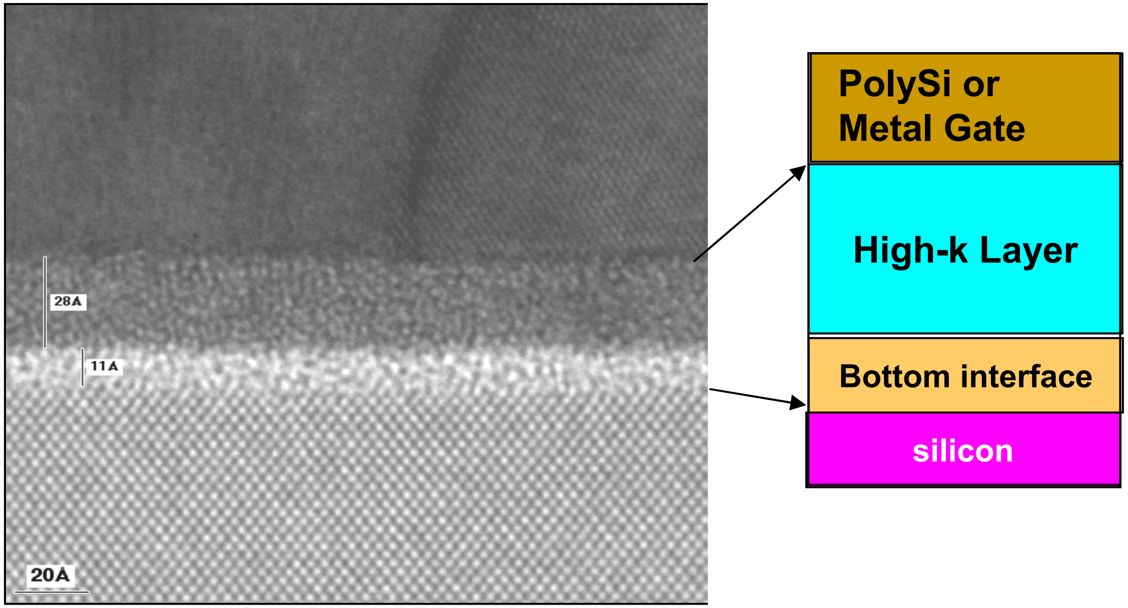
N throughout

N-implant

oxidation

more N at bottom

Methods to Reduce Gate Leakage: High-K

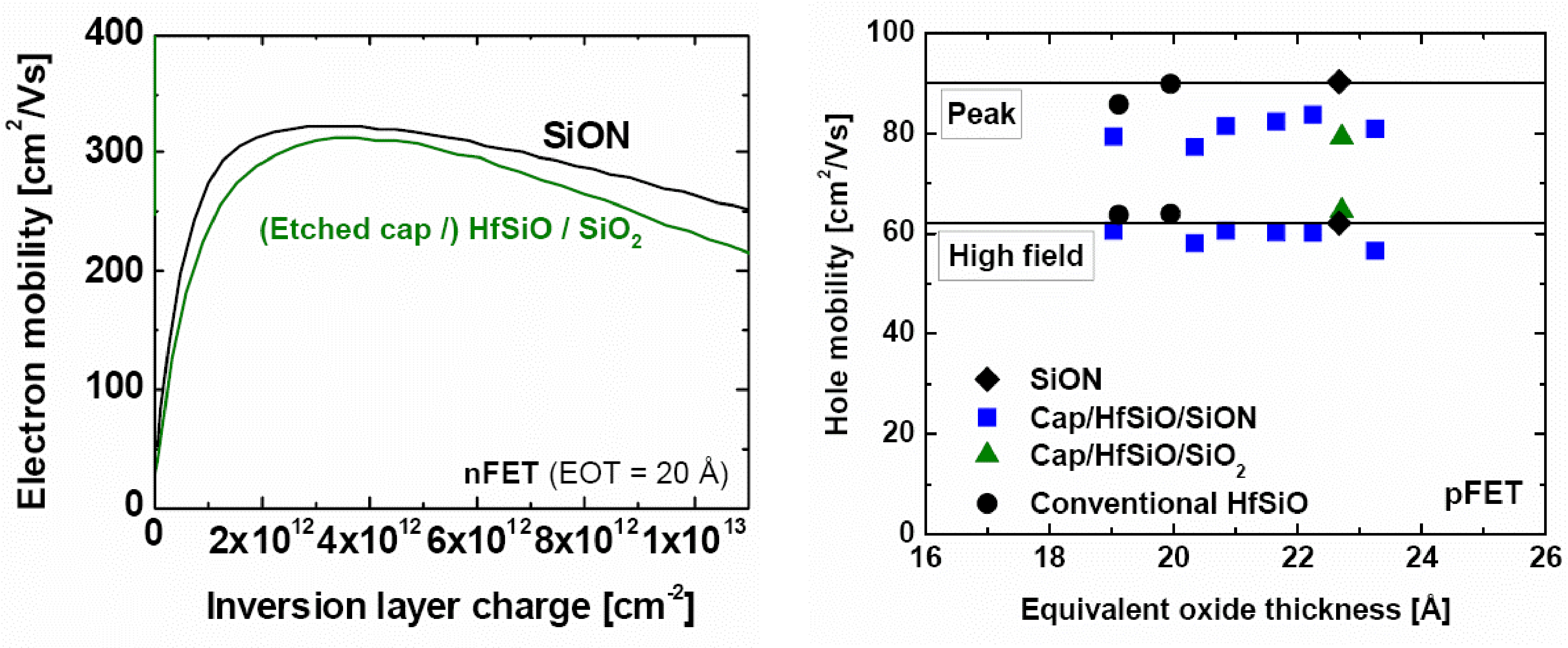


High-k/Metal Gate Stack: Tinv = 14.5A, ToxGL = 16A

Benefits	Issues
• >1000x lower IG • Lower Tinv at same IG to enable device scaling	• Vth control (WF engineering) • Charge trapping • Mobility degradation • Increased complexity

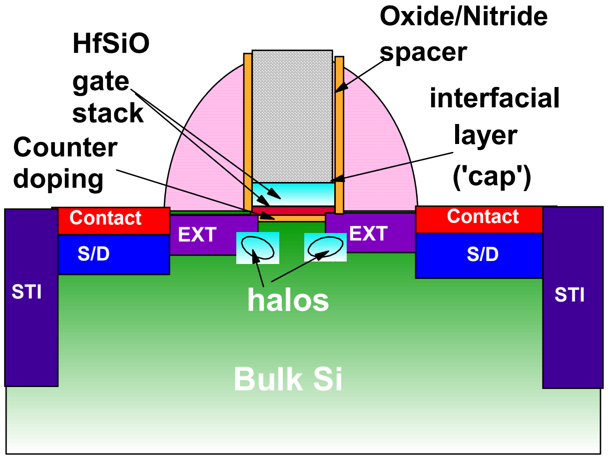
Mobility

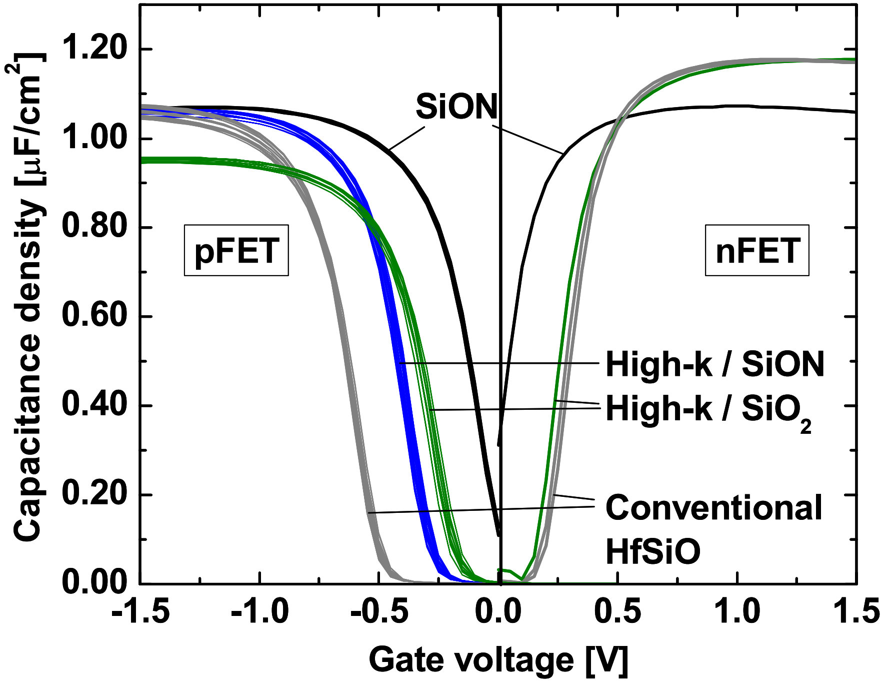
- Acceptable long channel mobility with Hf-based oxides
- Requires optimization of HfSiO(N)/SiO(N) composition



[*M Frank et al., VLSi-TSA05*]

Gate Workfunction Tuning

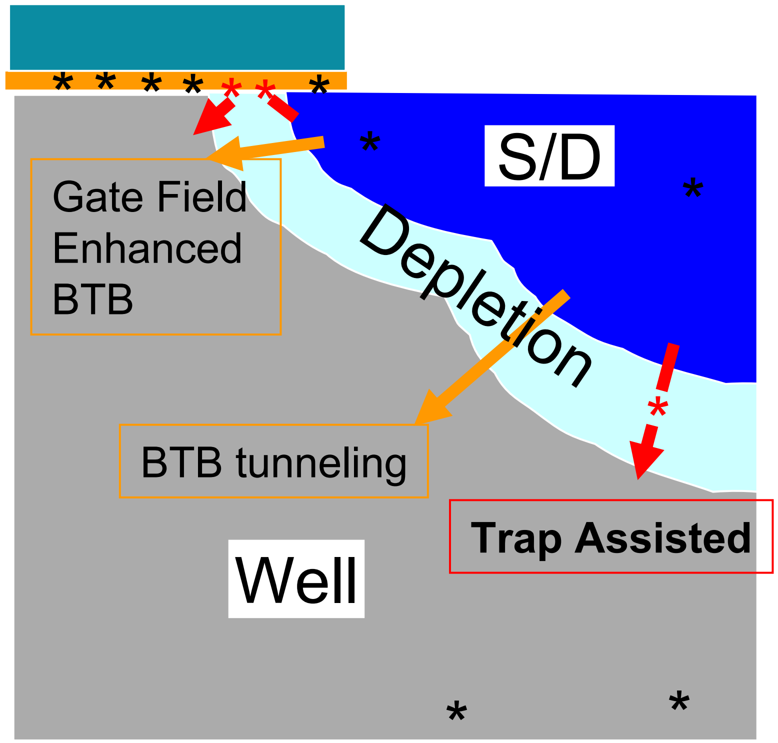




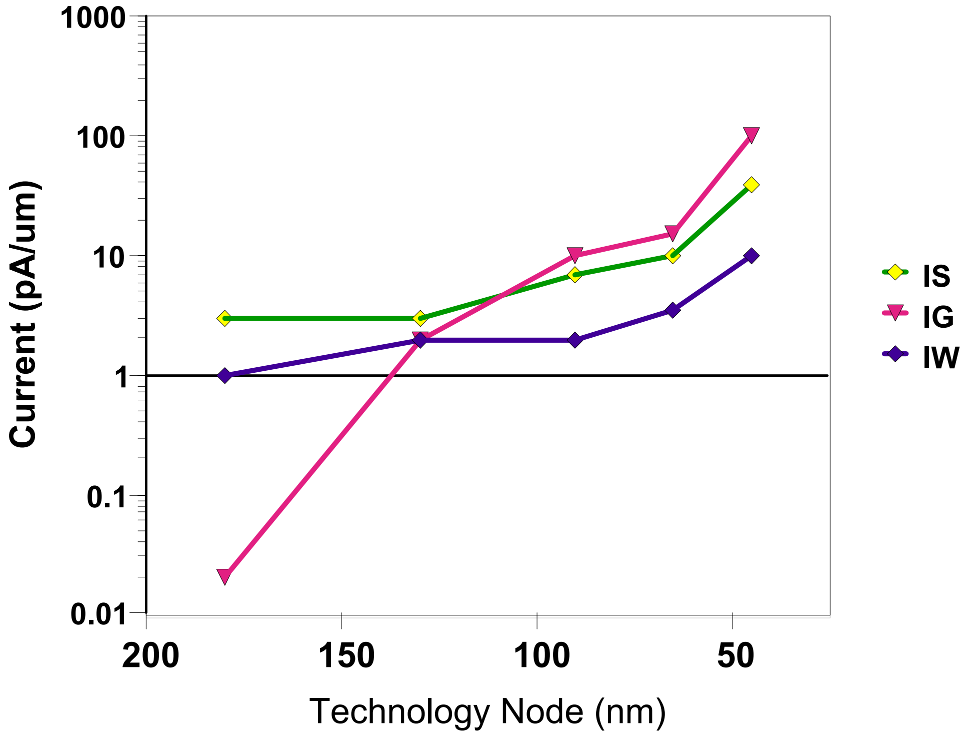
- ➢ Optimized high-k dielectric stack reduces pFET Vt shift by 200~300 mV
  - ➢ Selective use of ultra-thin interface/surface modification layers

M. M. Frank et al VLSI-TSA 2005

IW: Tunneling & Trap-Assisted Current



Schematic of IW sources

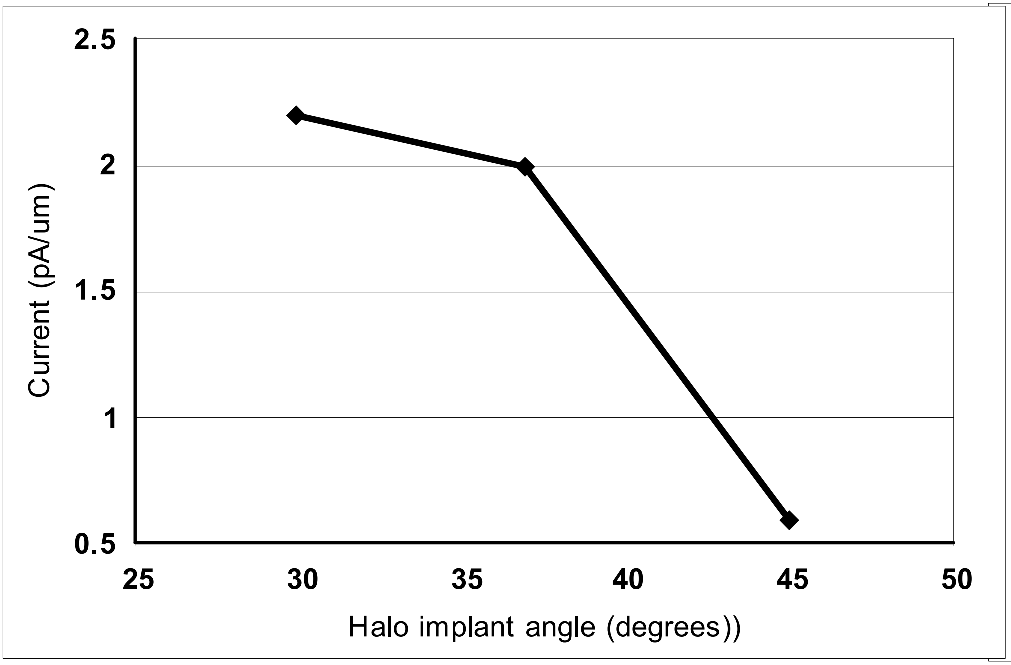


Relative Contribution of IW

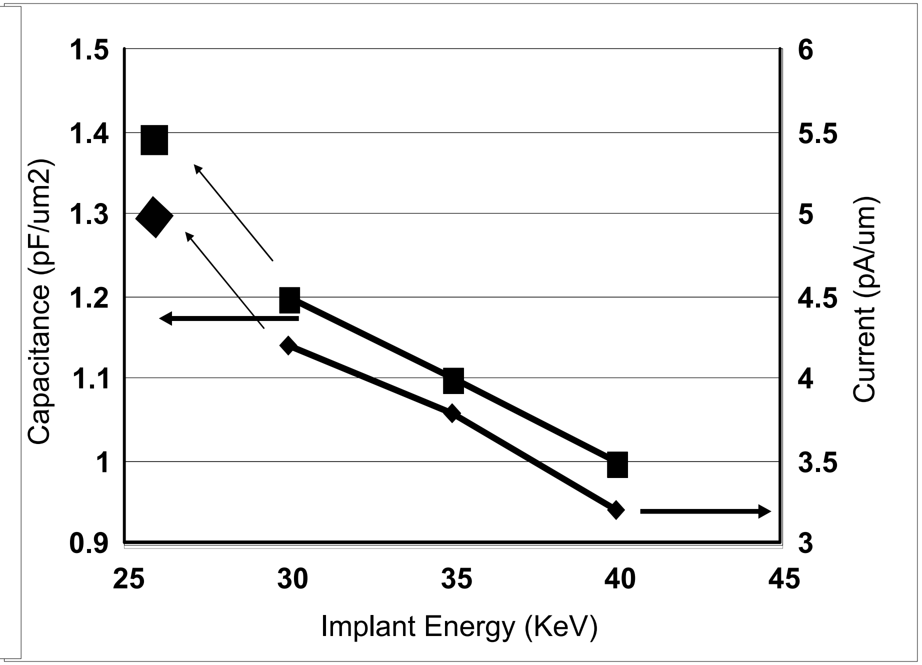
- Band to band tunneling increases with doping levels & steeper gradients
- Gate field enhanced tunneling increases with thinner gate dielectric
- Reduction of trap assisted current varies with cause

Methods to Reduce Junction Leakages

- Leakage modulated primarily by transistor doping profiles



NFET Junction Leakage vs. Halo Angle

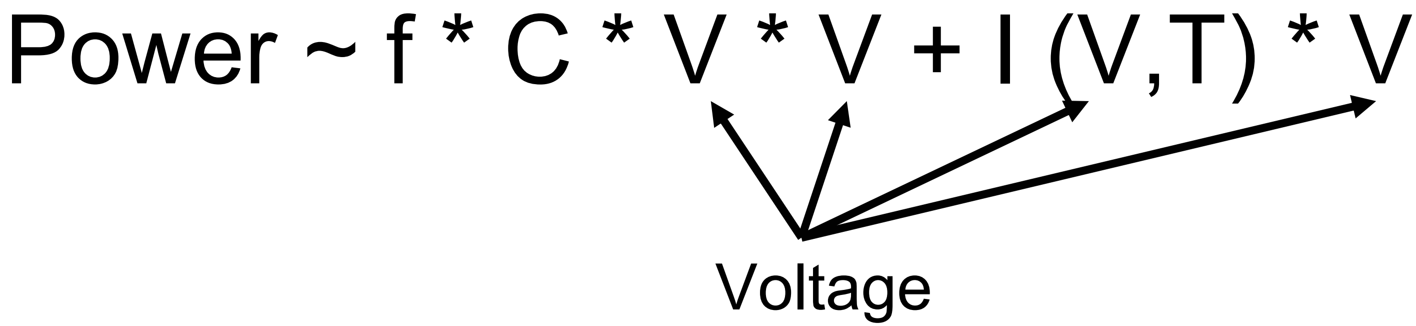


PFET Junction Leakage vs. S/D Energy

Ref: Hook, ACEED 2005

Low Active Power

Components of Active Power



$$\text{Power} \sim f * C * V * V + I\,(V,T) * V$$

Voltage

Higher Transistor Performance at Same Leakage

↓

Same Fmax at Lower Voltage

↓

Lower Active Power

Performance Scaling

Traditional performance scaling:

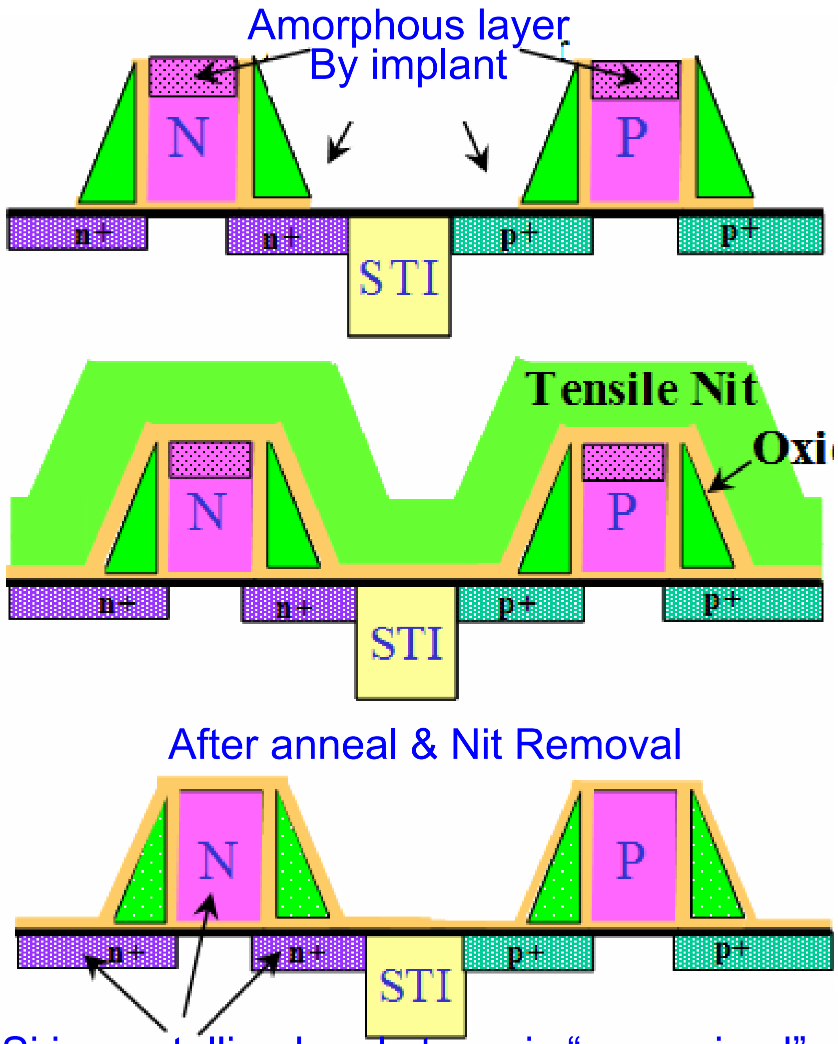
- Shorter Gate Length
- Higher Gate Capacitance (IG)
- Shallower Junctions (IW)
- Lower Threshold Voltage (IS)
- Lower Supply Voltage

All did not scale in 65nm technology

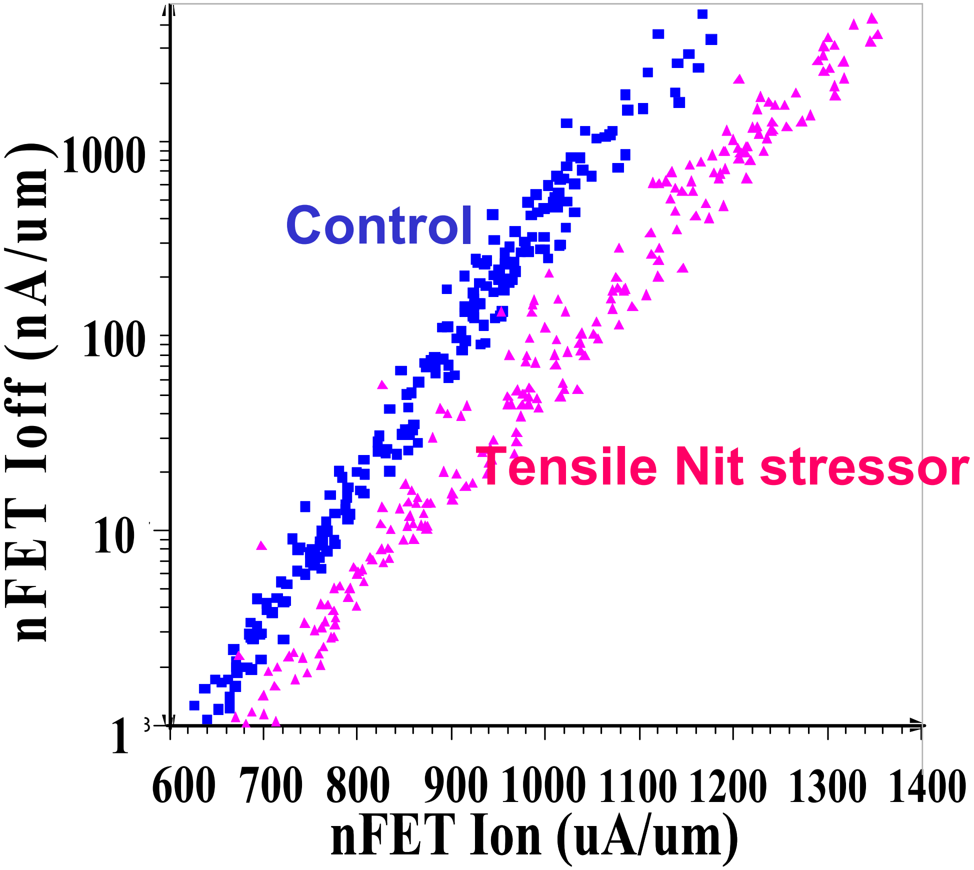
Higher performance with:

- Higher Supply Voltage
- Higher Inversion Capacitance
- Higher Mobility

Mobility Innovation: Stress Memory

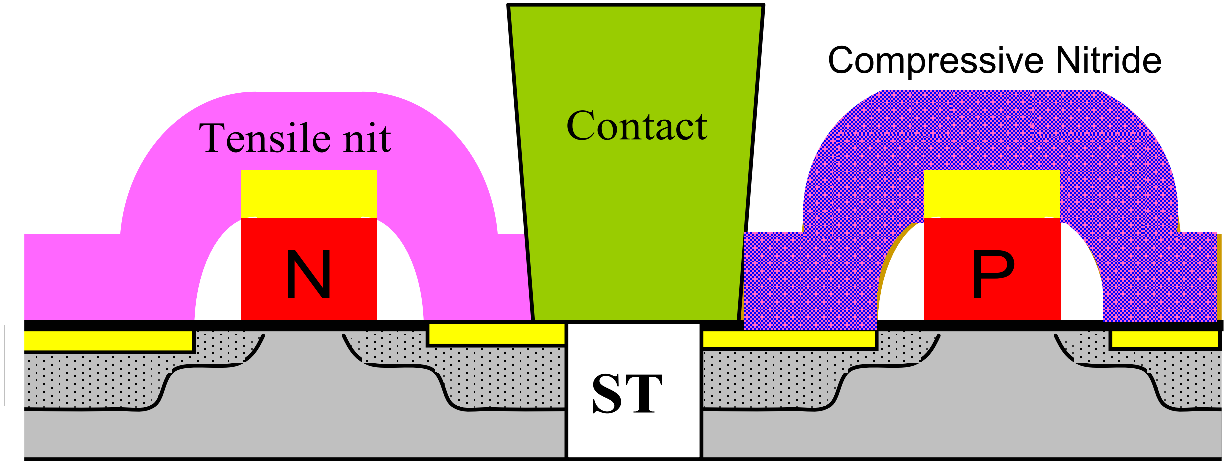


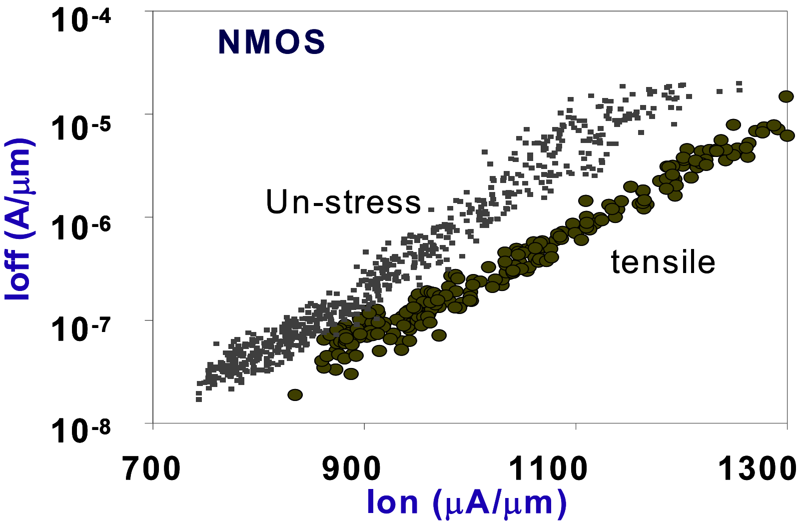
Si is crystallized and stress is “memorized”

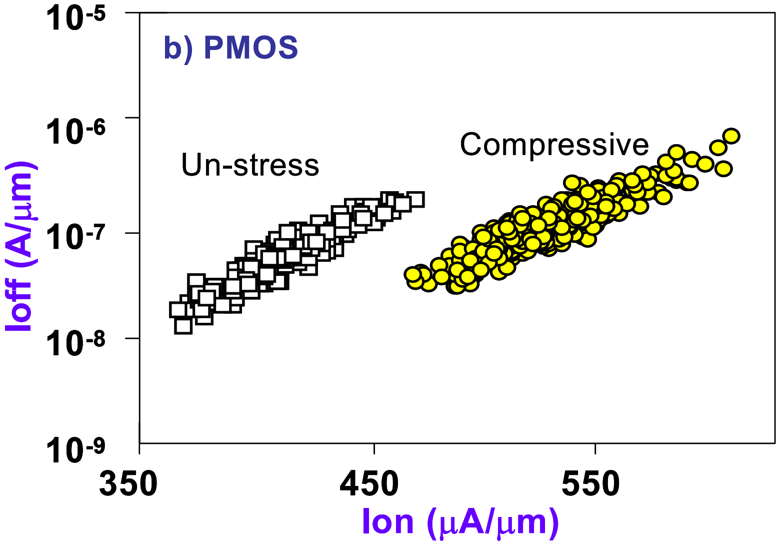


[Chan, CICC ’05]

Mobility Innovations: Strained Liner

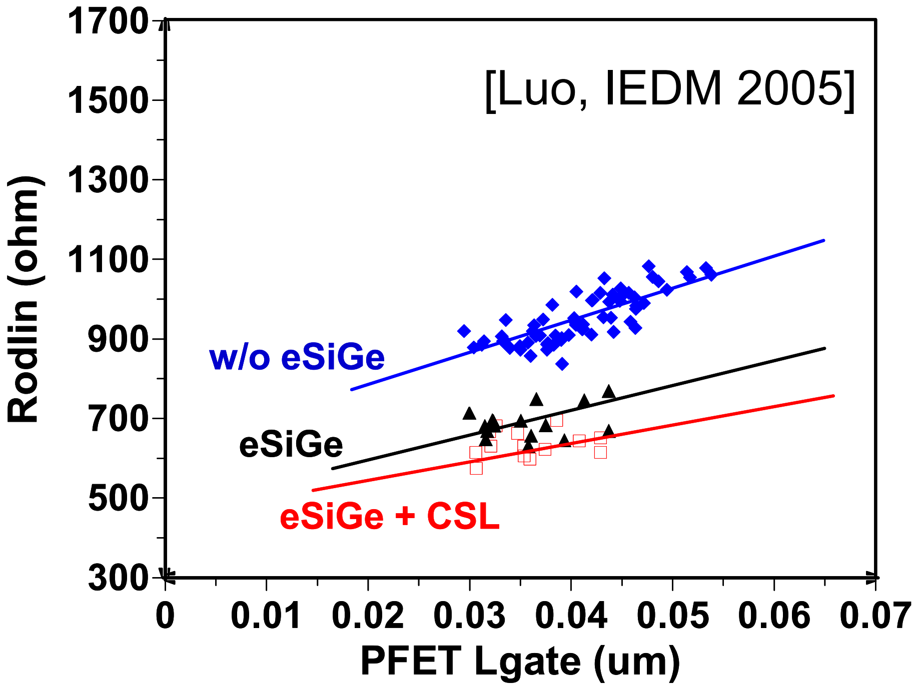




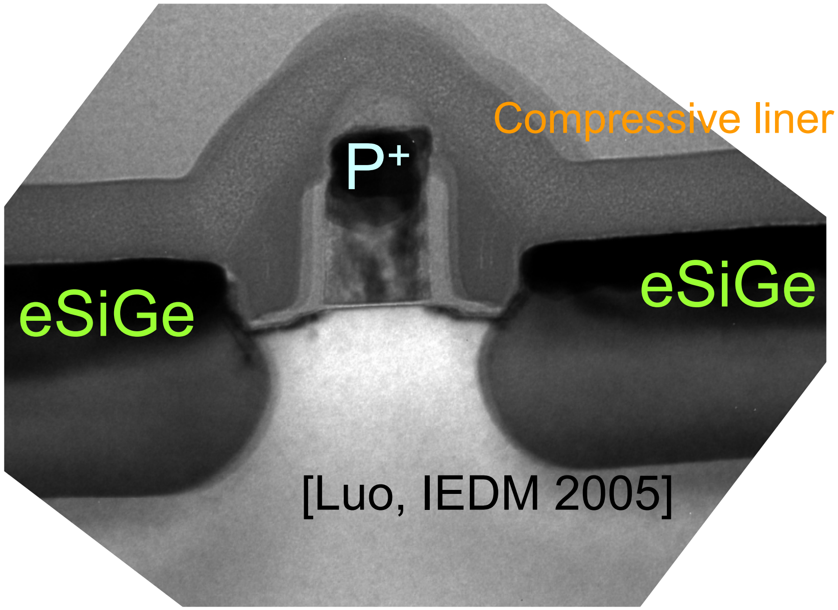


[Chan, CICC ’05]

Mobility Innovations: Embedded SiGe



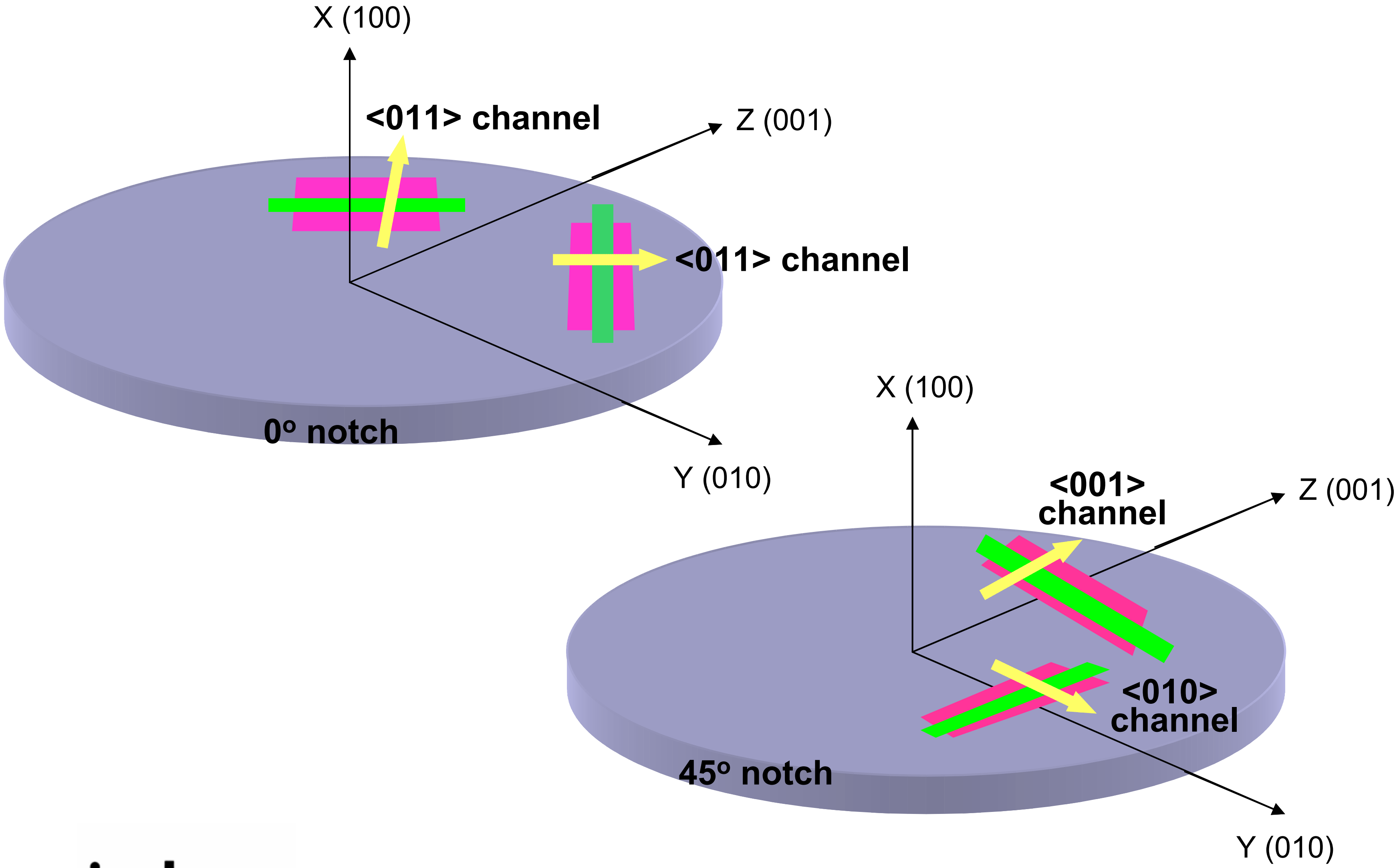
PFET Liner Mobility Enhancement



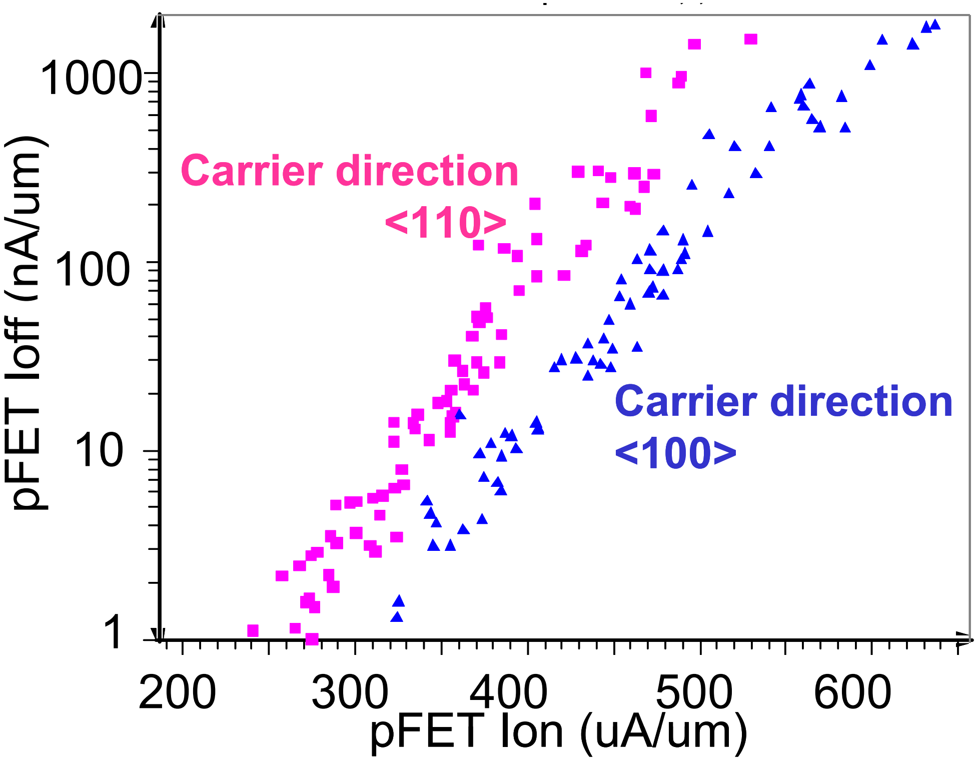
Embedded SiGe Cross-section

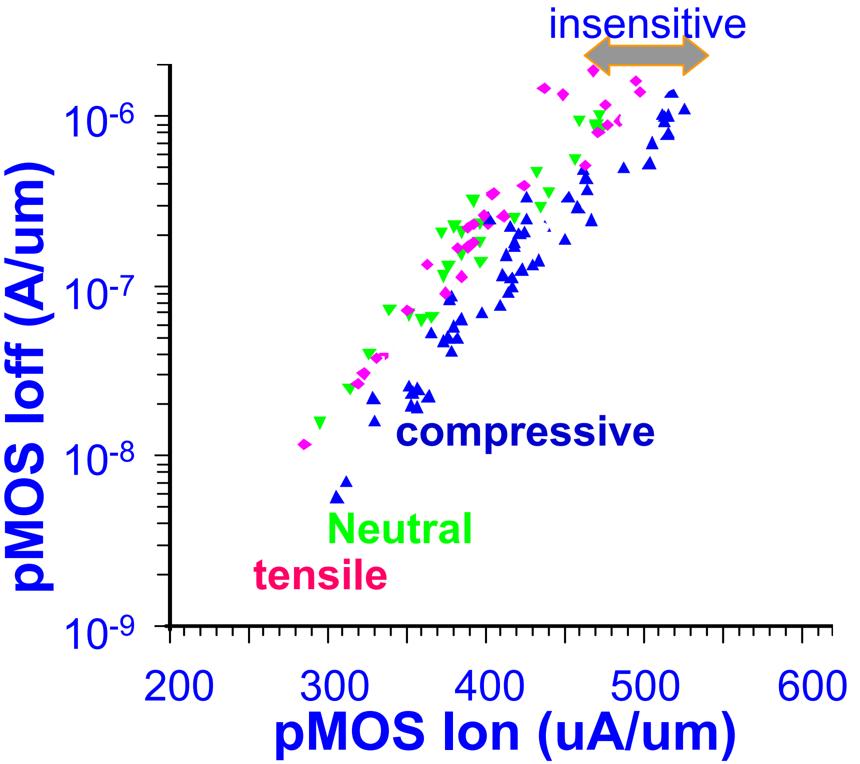
- **Introduces compressive stress**
- **Lowers contact resistance**

Mobility Innovations: <100> PFET



Mobility Innovations: <100> PFET

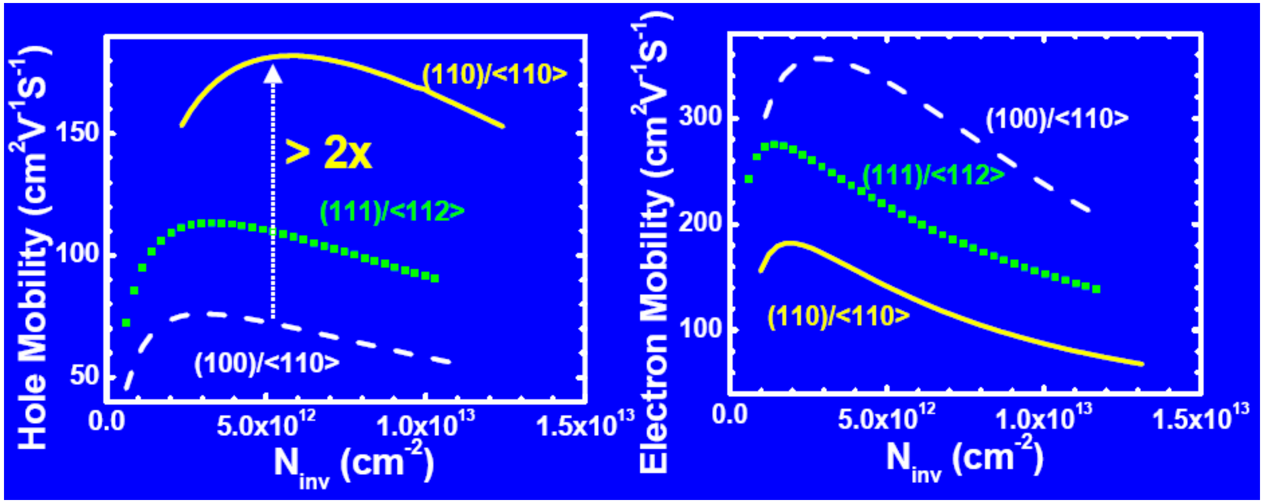




[Chan, CICC '05]

- Significant boost in PFET current without added process steps
- Loss of ability to increase current with compressive stress

Mobility Innovations: Hybrid Orientation



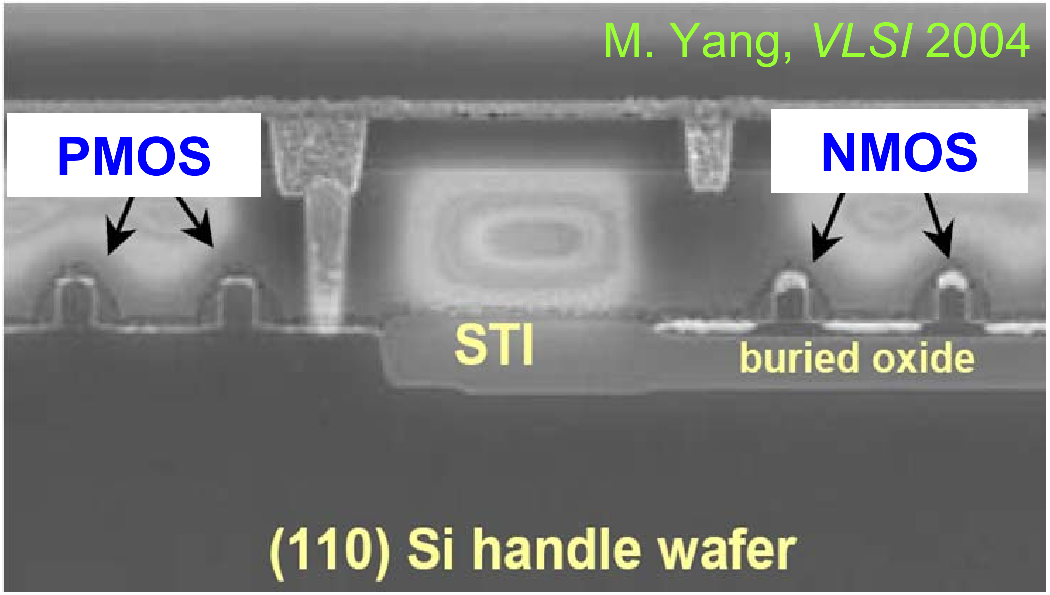
- 110 surface:

  2x higher PFET μ

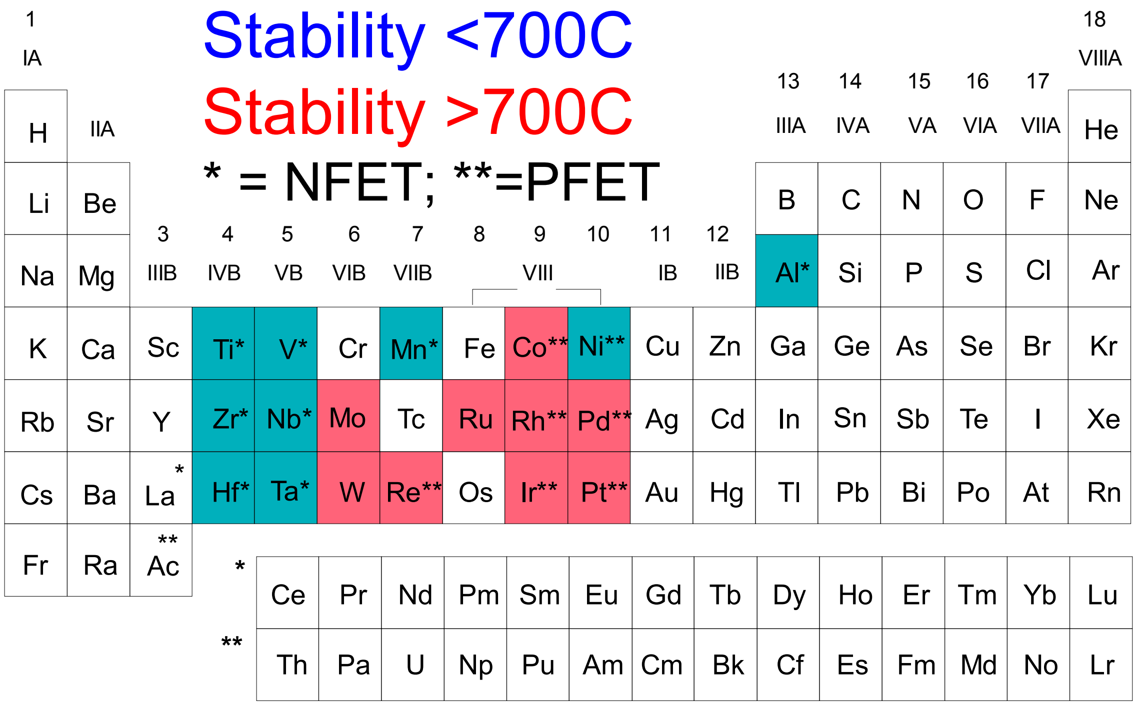
  >2x lower NFET μ

- Hybrid Orientation
  - 110 for PFET
  - 100 for NFET

Process Challenges:
- Low defect epitaxy
- Planarization
- Trench isolation


M. Yang, *VLSI* 2004

Inversion Capacitance: Metal Gates



Stability <700C

Stability >700C

* = NFET; **=PFET

1 IA	IIA	3 IIIB	4 IVB	5 VB	6 VIB	7 VIIB	8	9 VIII	10	11 IB	12 IIB	13 IIIA	14 IVA	15 VA	16 VIA	17 VIIA	18 VIIIA
H																	He
Li	Be											B	C	N	O	F	Ne
Na	Mg											Al*	Si	P	S	Cl	Ar
K	Ca	Sc	Ti*	V*	Cr	Mn*	Fe	Co**	Ni**	Cu	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Sr	Y	Zr*	Nb*	Mo	Tc	Ru	Rh**	Pd**	Ag	Cd	In	Sn	Sb	Te	I	Xe
Cs	Ba	* La	Hf*	Ta*	W	Re**	Os	Ir**	Pt**	Au	Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra	** Ac															

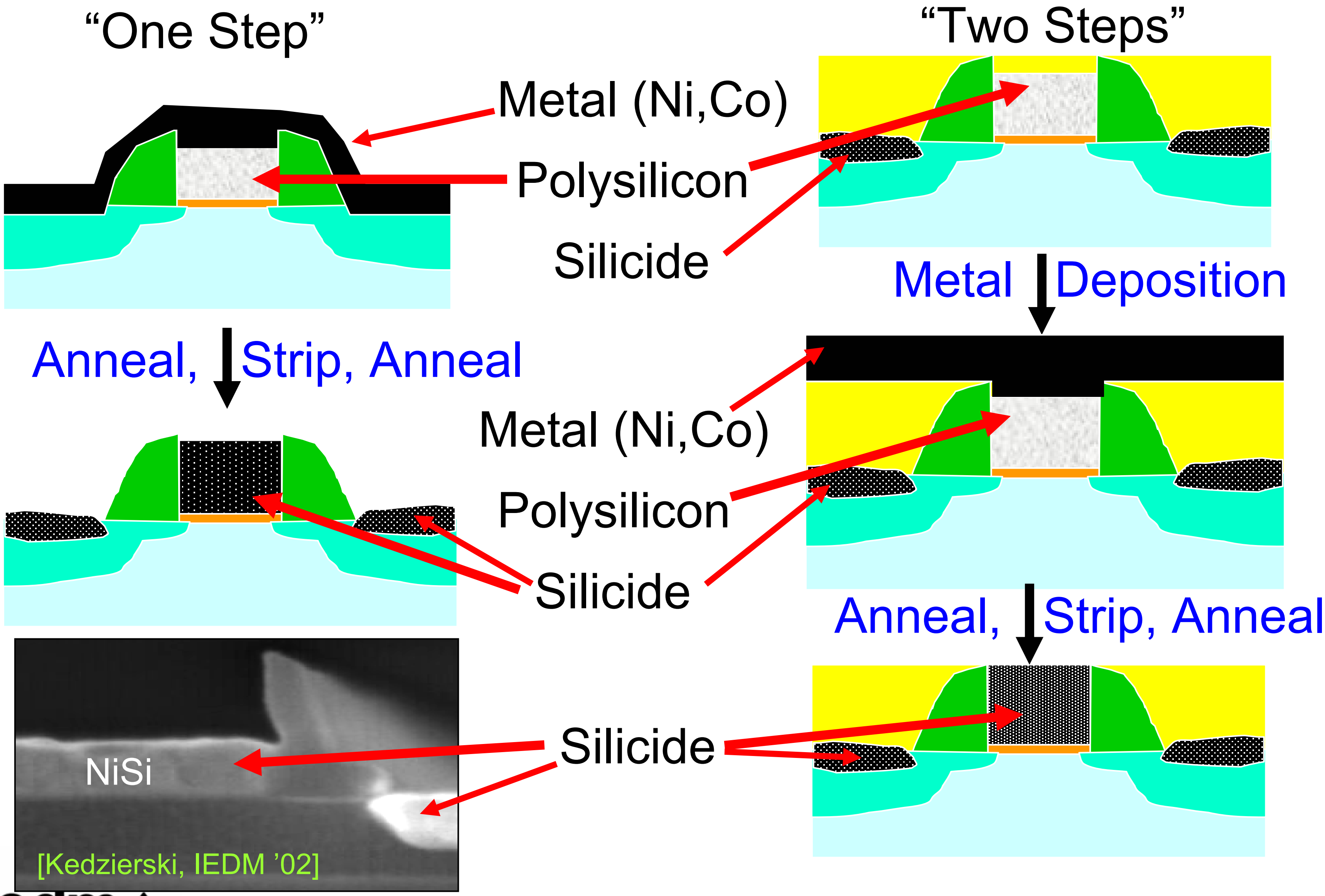
*	Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
**	Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr

Metals 3-5 nm thick on 500 nm SiO_2, anneal 3 °C/s up to 1000 °C in FG

Binary/ternary alloys: W_2N*, Ta_2N*, TaN*, TaSiN*, RuO_2**, $CoSi_2$, NiSi

- Metal gate incorporation to remove gate depletion
- Holy Grail: Band edge workfunction & thermally stable

Metal Gate Integration Options: FuSi



“One Step”

“Two Steps”

Metal (Ni,Co)

Polysilicon

Silicide

Metal Deposition

Anneal, Strip, Anneal

Metal (Ni,Co)

Polysilicon

Silicide

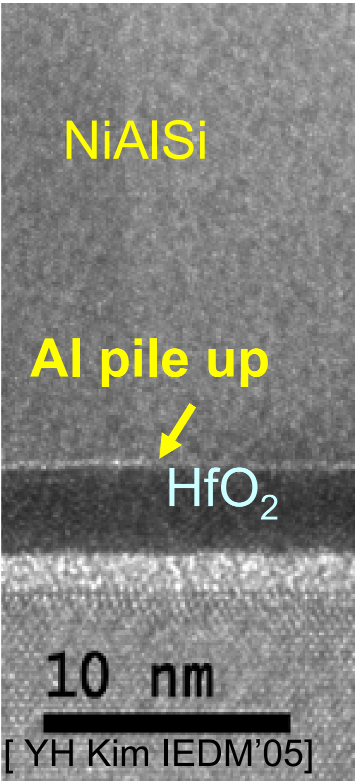
Anneal, Strip, Anneal

Silicide

[Kedzierski, IEDM ’02]

Challenges for FuSi

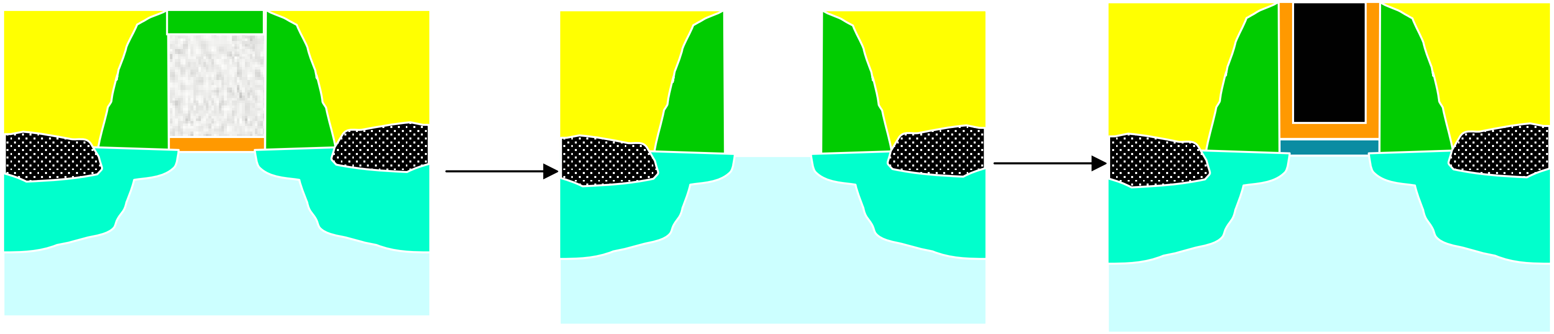
- **Dual Workfunction creation**
  - **Alloys**
  - **Doping**
  - **Phase change**



[YH Kim IEDM'05]

- **Workfunction control & stability**
- **Variation with gate density & size**

Metal Gate Integration Options: Replacement Gate



Build Device

Etch Gate

Deposit High-k
Deposit Gate Metal
Deposit Fill Metal
CMP

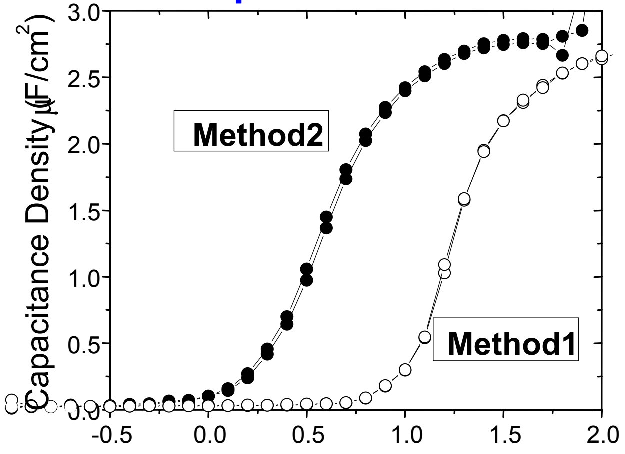
Challenges:

- Integration of different workfunction metals: high complexity
- High-k deposition on small gate area
- ALD probably required for gate metal

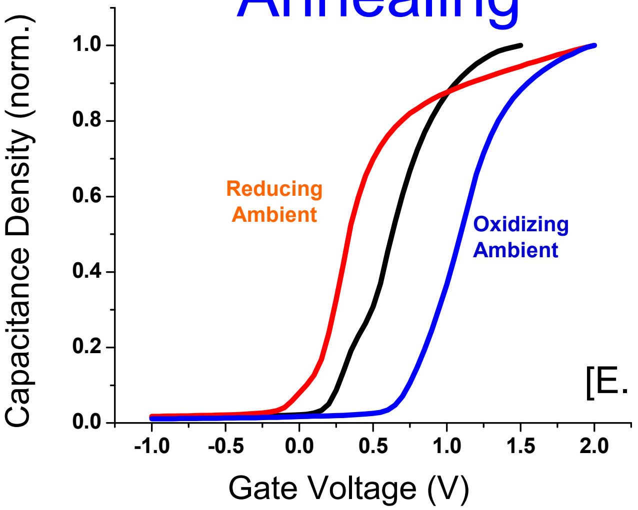
Metal Gate Workfunction Stability

- Workfunction of integrated metal gates has strong dependence on deposition & annealing conditions

Deposition



Annealing

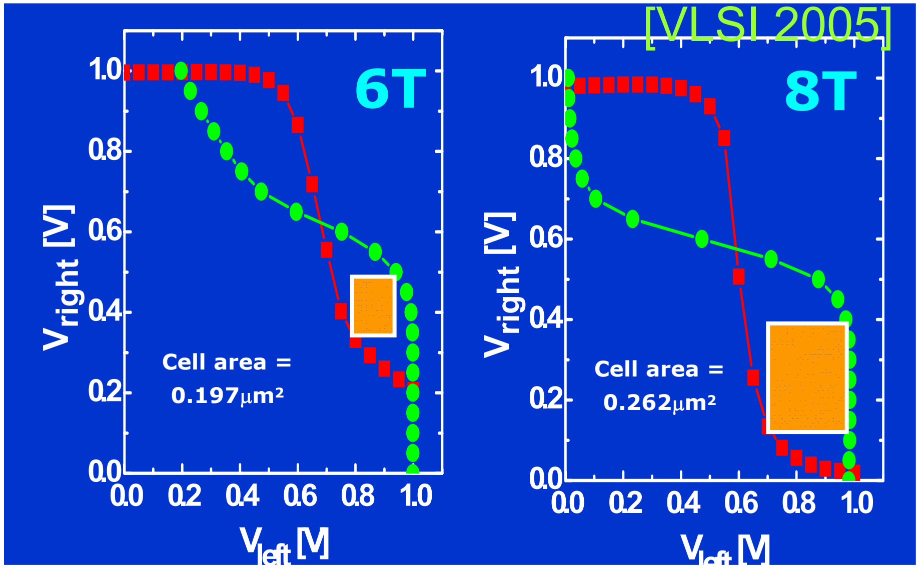


[E. Cartier, VLSI '05]

- Potential root causes of workfunction shifts
  - Metal induced gap states (MIGS)
  - Oxide charge (O vacancies) in HfO_2
  - Oxidation of interfacial metal
  - Hf-diffusion into metal (WF change)
  - Dipole layers at SiO_2/HfO_2 interface

Memory Limitation to Voltage Scaling

- SRAM cell stability limits scaling of array Vdd
  - Vth mismatch due to dopant fluctuation in best case is constant with scaling
    - Lack of gate dielectric scaling has caused it to increase
  - Reduction of all other components of mismatch critical



Butterfly curve comparison for scaled cells

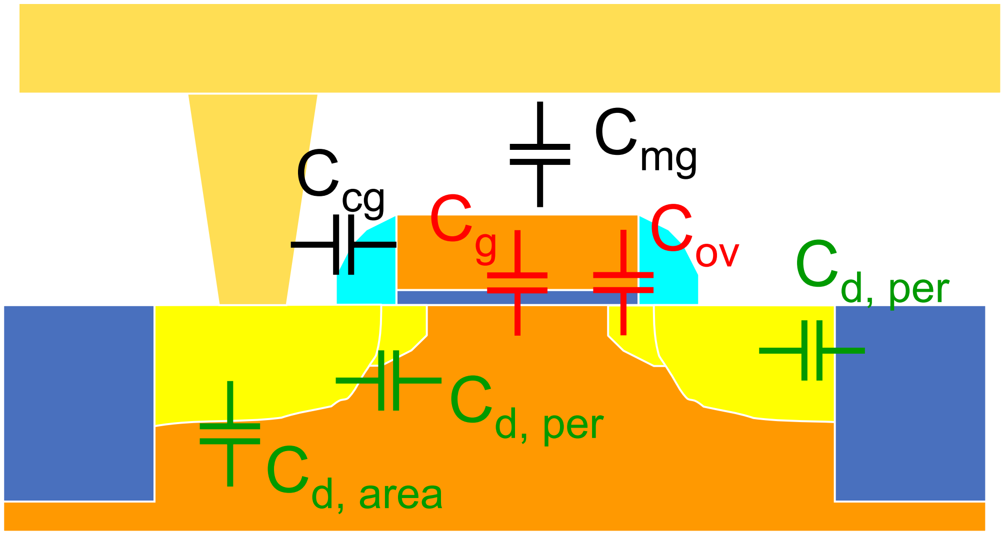
- Design Options
  - Larger cells
  - Separate array Vdd
  - Alternative cells/memory
    - 8T SRAM
    - eDRAM

Components of Switching Power

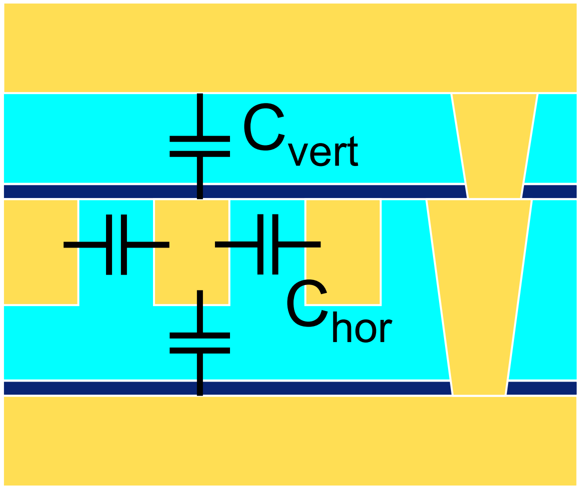
$$\text{Power} \sim f * C * V * V$$

Capacitance

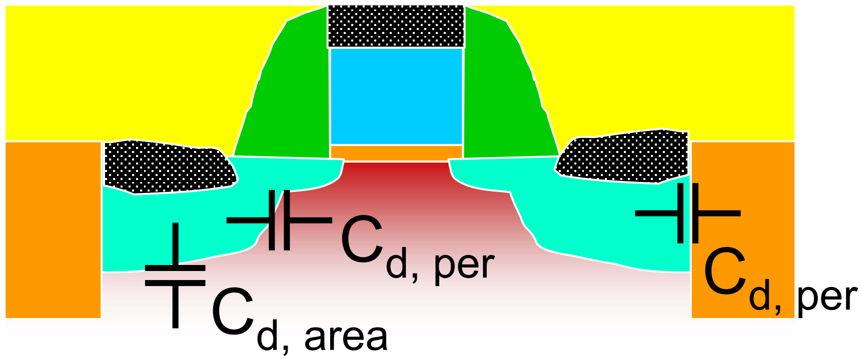
Transistor



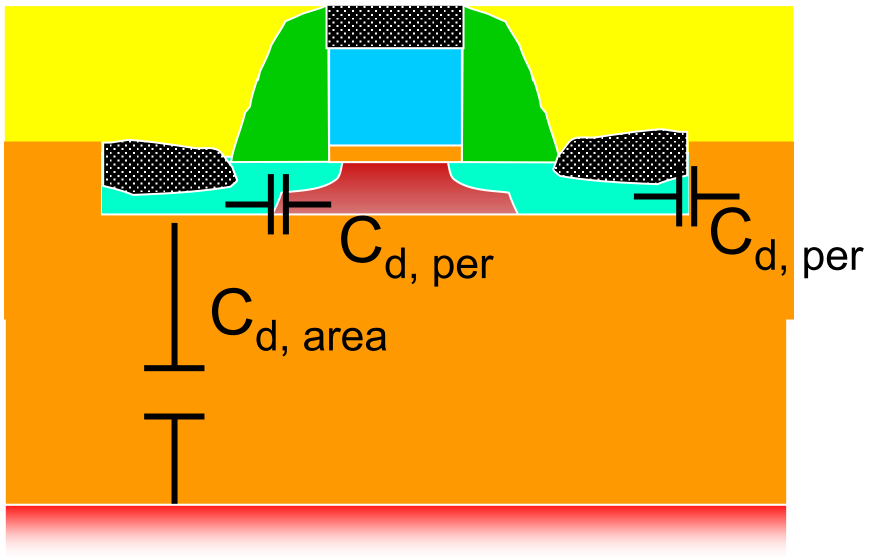
Metallization



Capacitance Reduction: SOI



Bulk Transistor



SOI Transistor

- Reduction of area diffusion capacitance to negligible level
- Reduction of perimeter capacitance with film scaling

- Additional AC drive current benefit from gate coupling

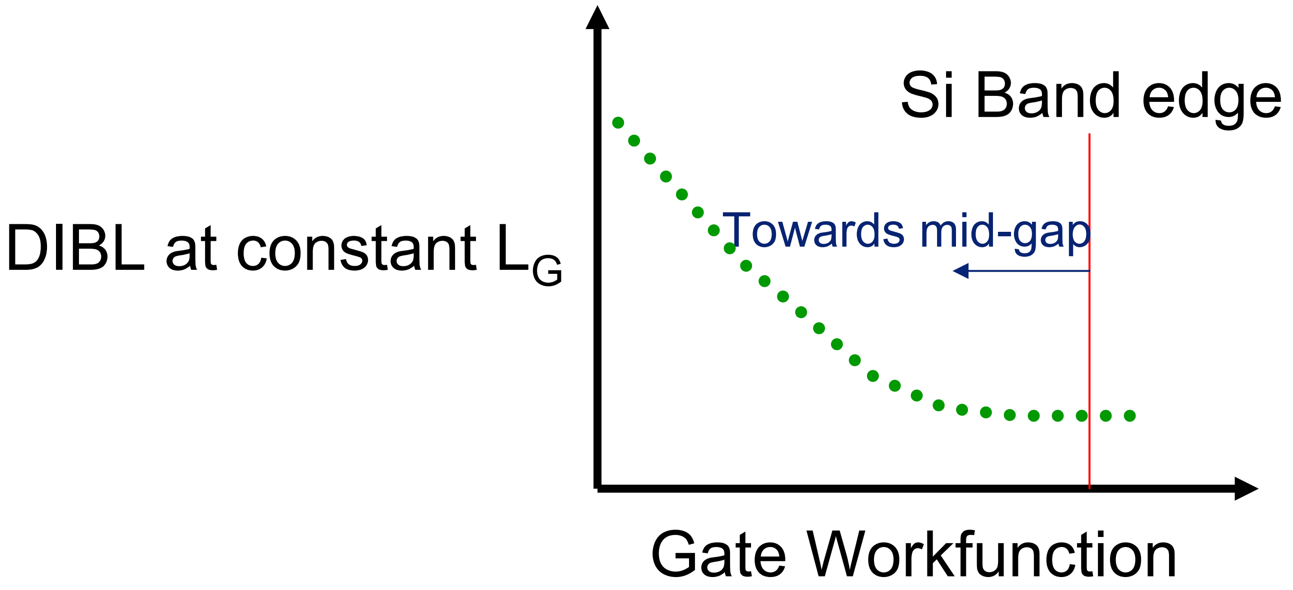
Options to Gate Capacitance Scaling

- Need better electrostatic control to scale L_G
  - Higher gate inversion capacitance
    - High-K gate dielectric material to reduce EOT
    - Metal gate material to eliminate gate depletion
  - Fully depleted double gate structures
    - Better channel control through structural change

- L_G must decrease more than C_{inv} increases

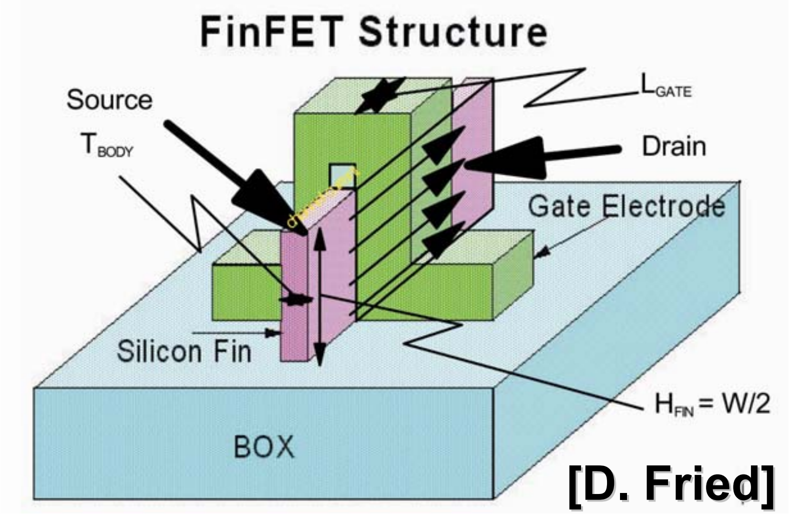
Capacitance Scaling with Metal Gate

- **L_G must decrease to prevent capacitance increase**

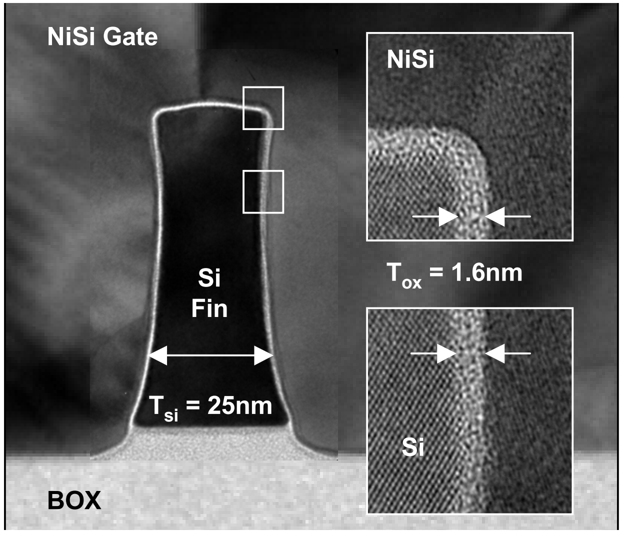


- **Short channel effect degradation when metal gate workfunction deviates too far from band edge**
  - **Lose portion of performance benefit and most of power benefit**

One Double Gate Structure: FinFET



[D. Fried]

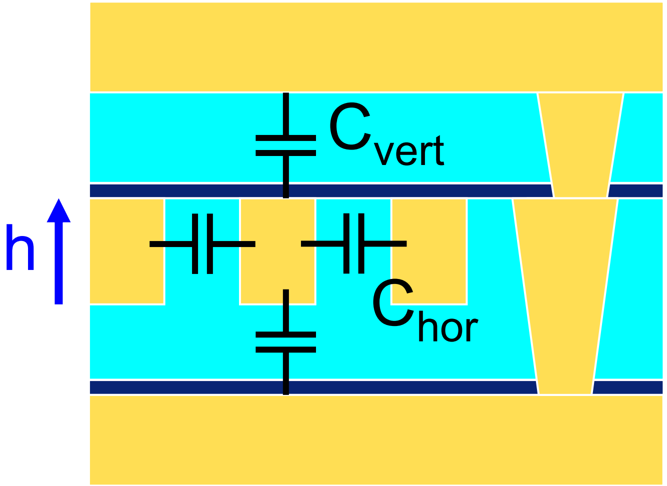


Kedzierski, IEDM 03

Process Challenges:

- Fin creation and control
- Source/drain resistance engineering
- Contact formation and control

BEOL Capacitance Scaling



Performance ~ R * C

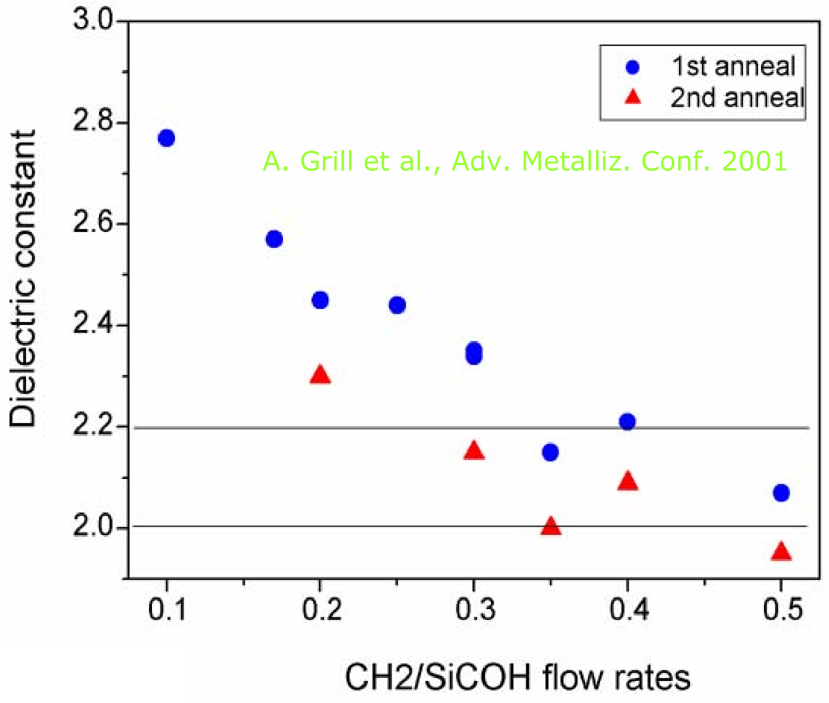
Capacitance ~ k_{eff} * h / space

Resistance ~ ρ / (h * w)

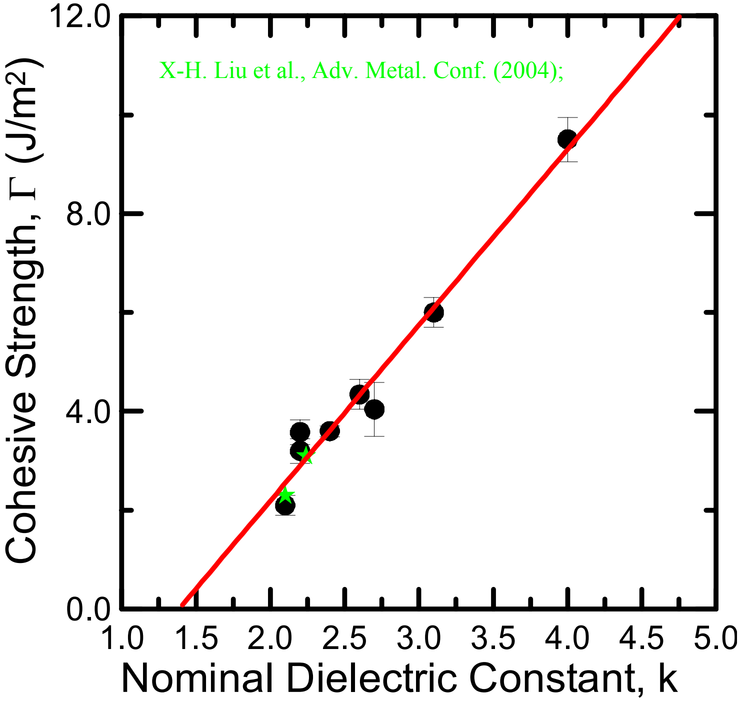
Reduce inter-level dielectric constant => lower capacitance

Reduce resistance => lower height => lower capacitance

Capacitance Scaling: Reducing BEOL k



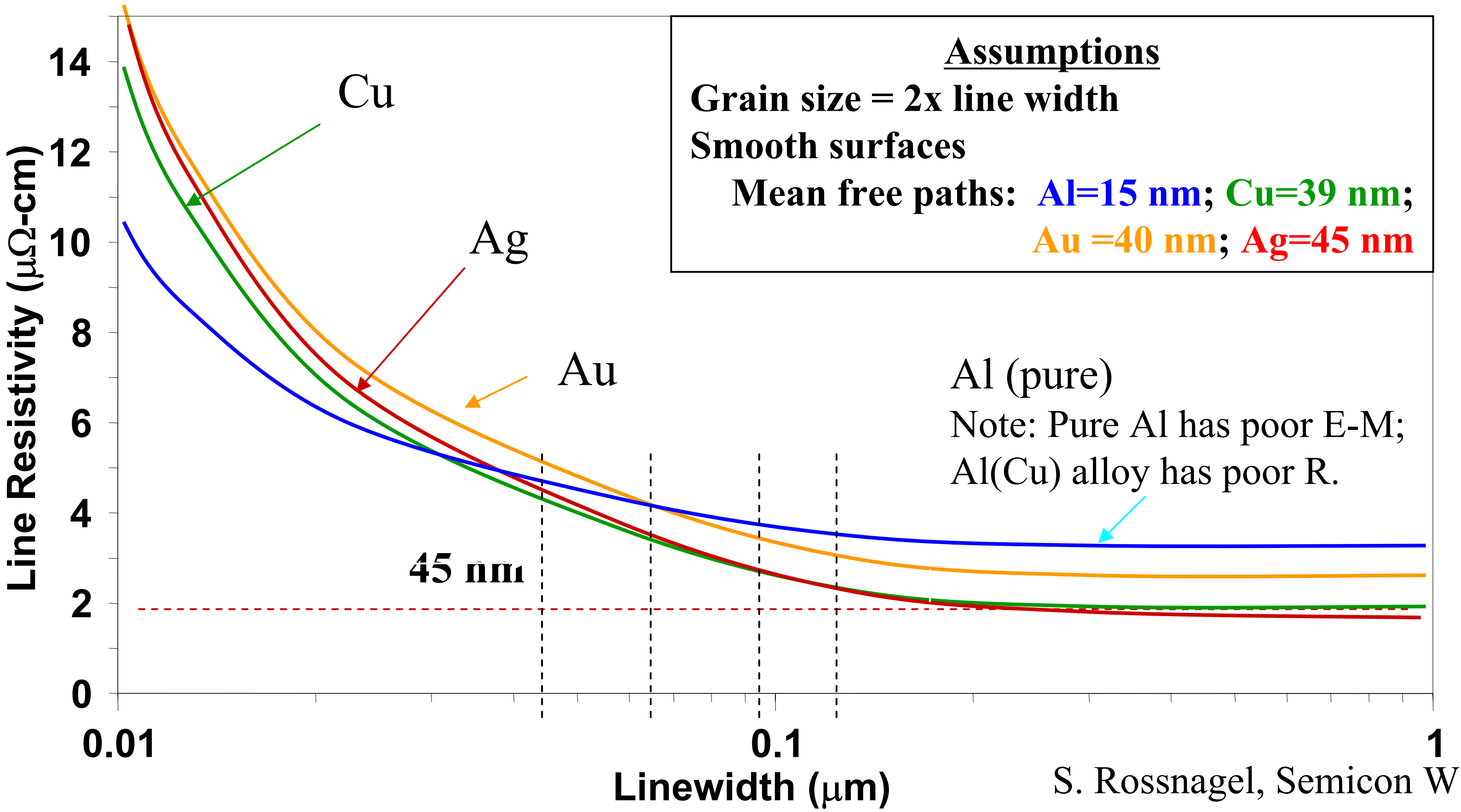
A. Grill et al., Adv. Metalliz. Conf. 2001



X-H. Liu et al., Adv. Metal. Conf. (2004);

- Multiple porous dielectric options with $k < 2.4$
  - Spin-on and CVD deposition options
- All materials have lower material strength as k decreases
  - Optimization of BEOL stack & packaging required

Capacitance Scaling: Scaling h



Assumptions

Grain size = 2x line width

Smooth surfaces

Mean free paths: Al=15 nm; Cu=39 nm; Au =40 nm; Ag=45 nm

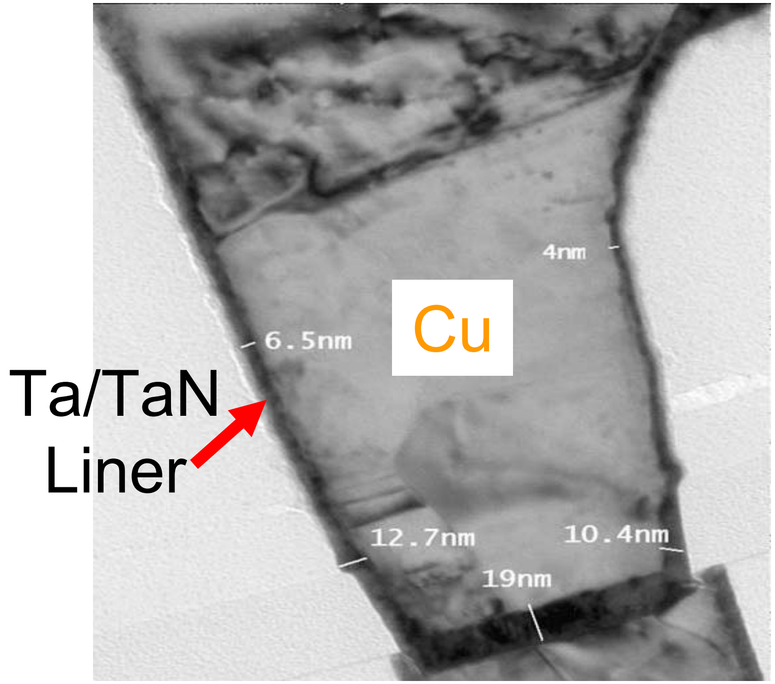
Al (pure)

Note: Pure Al has poor E-M;
Al(Cu) alloy has poor R.

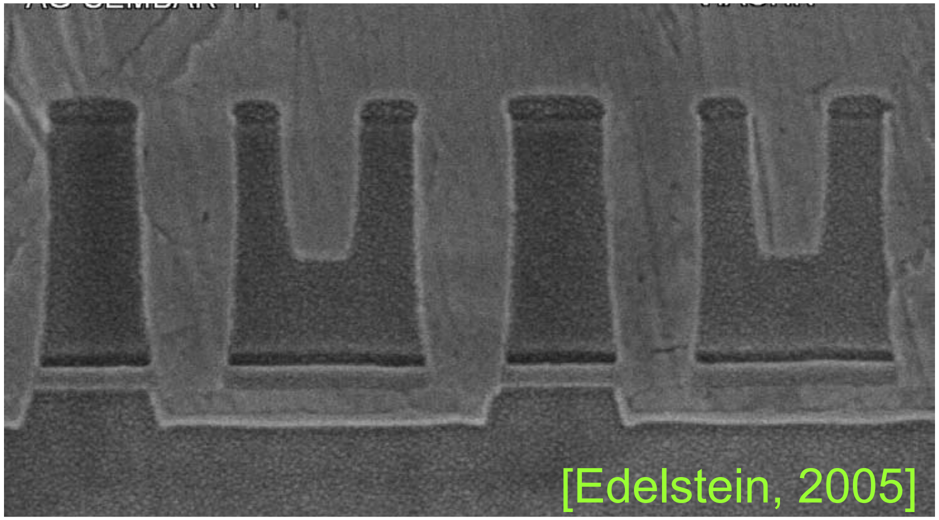
S. Rossnagel, Semicon West (2004).

- Copper will continue to be material for low ρ metallization

Capacitance Scaling: Scaling h



ITRS 45nm PVD liners demonstrated

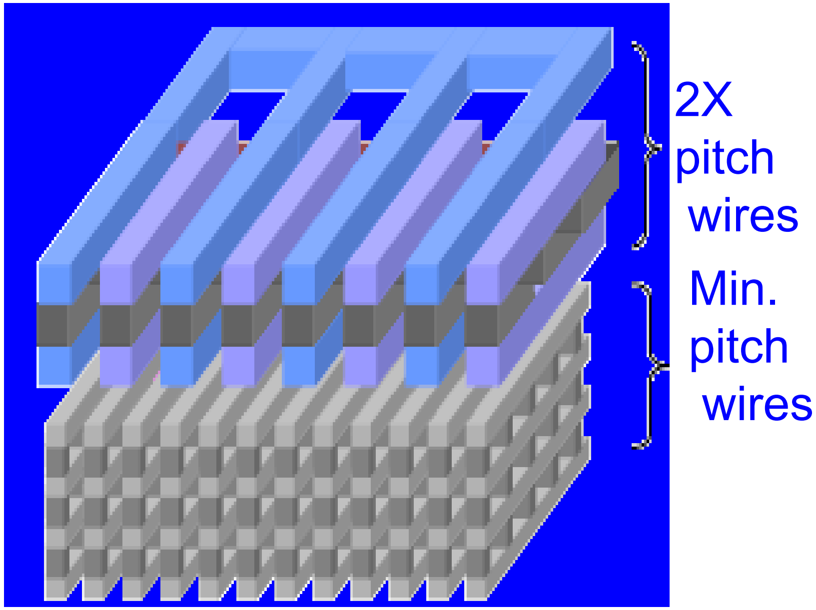

[Edelstein, 2005]

Cu BEOL using Ru liner

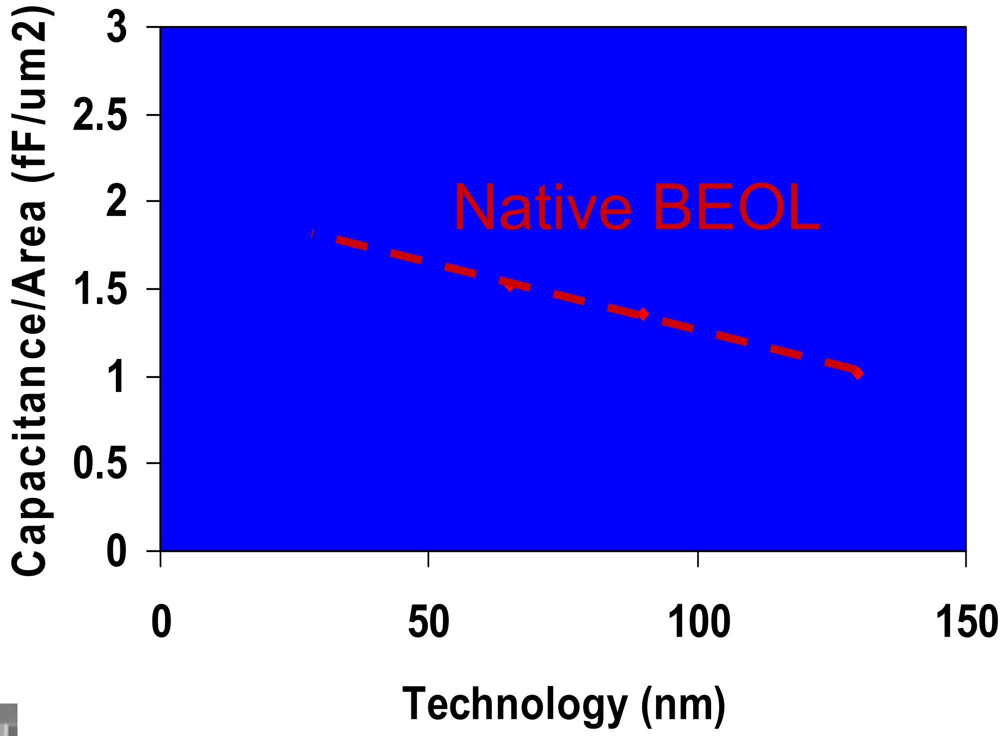
- **Scaling requires thinner liner & seed films**
  - **45nm dimensions demonstrated**
  - **Porous dielectrics must be compatible with thin liner to have benefit**

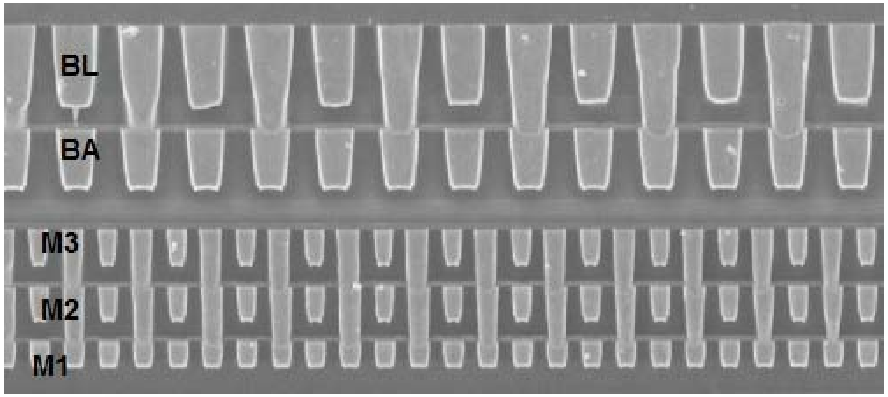
- **ALD liner & Cu seed reduction provide opportunity for additional scaling**

Passives Scaling: BEOL Capacitors



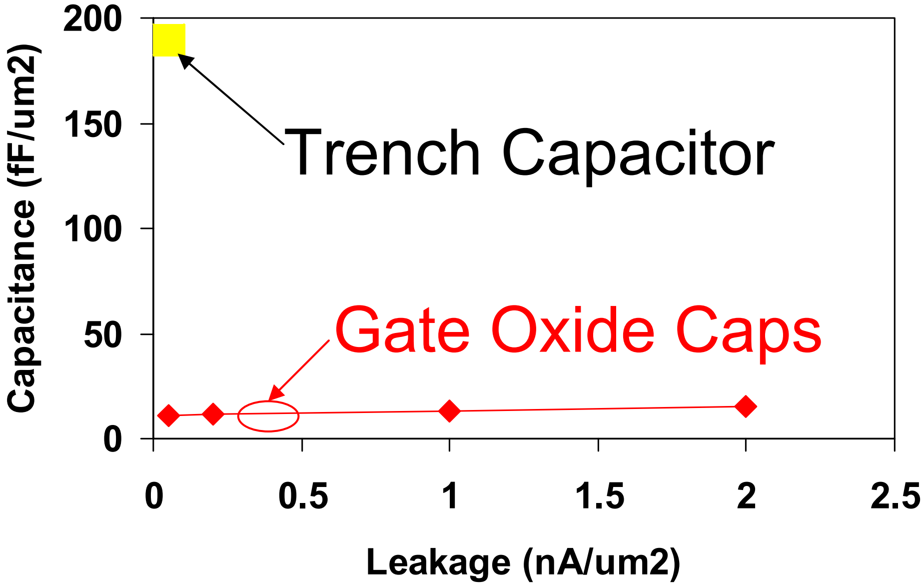
Native BEOL capacitor

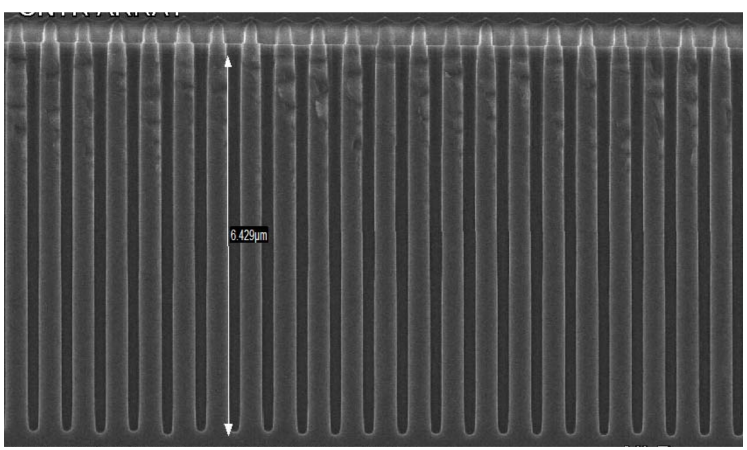




- Benefit of scaling:
  better “free” BEOL capacitors
- Good tolerance due to averaging over many levels

Passives Scaling: Decoupling Capacitors





Trench Capacitors

- Gate capacitor scaling not possible with low passive power
- >10x reduction in area & >100x reduction in leakage with trench capacitors

Conclusions: Handheld Low Power

- Standby power dominated

- Choices:
  - Add strain engineering without gate scaling
  - Add high-K dielectrics to enable gate scaling
  - Add design complexity to modulate leakage

- Decision will be driven by lowest cost solution

Conclusions: Plugged In Low Power

- Active Power Dominated
- Performance elements added as developed

- Choices:
  - Lower supply voltage
    - May require new memory choice
  - Add design complexity to reduce both switching and passive power
    - Voltage islands, clock gating, etc…